Automotive 2.5G/5G/10GBASE-T1 Ethernet Transceiver

Overview

Features

The BRIGHTLANE™ Q3241, BRIGHTLANE™ Q3242, and BRIGHTLANE™ Q3244 devices are single-port multi-gigabit Ethernet physical layer transceivers (PHYs) that support operation over a single-pair shielded twisted pair (STP) cable.

The BRIGHTLANE™ Q3241/Q3242/Q3244 BGA devices are pin-compatible, multi-gigabit, single-port PHYs housed in a 7 mm x 11 mm package that supports one, two, and three network rates respectively.

The BGA package device supports a multi-rate SerDes for direct connection to a MAC/switch port. The SerDes operates at 2.5/5/10 Gbps over a two differential pairs, reducing power and number of I/Os used on the MAC interface.

The BRIGHTLANE™ Q3241 device is also available in a 7mm x 7mm QFN package, which supports 2.5GBASE-T1 line and 2.5/5/10G system connections.

The devices integrate media dependent interface (MDI) termination resistors into the PHYs. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components.

The devices support 1.8V, 2.5V, and 3.3V LVCMOS I/O standards.

The devices incorporate the Advanced Virtual Cable Tester (VCT) feature, which uses time domain reflectometry (TDR) technology for the remote identification of potential cable malfunctions, reducing equipment returns and service calls. Using VCT, the devices will also detect cable opens, shorts, or any impedance mismatch in the cable and report the distance to the fault.

The devices use advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction. The devices achieve robust performance and exceeds electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

Note: For the remainder of this datasheet, the term devices is used interchangeably to represent the BRIGHTLANE™ Q3241,BRIGHTLANE™ Q3242, or BRIGHTLANE™ Q3244 products, unless a distinction is made based on the specific package or supported features.

- General
  - Single-port 2.5G/5G/10GBASE-T1 Ethernet transceiver, IEEE 802.3ch-2020 compliant
    - BRIGHTLANE™ Q3241 (BGA and QFN packages)
      - Supported line rate: 2.5GBASE-T1
    - BRIGHTLANE™ Q3242 (BGA package only)
      - Supported line rates: 5GBASE-T1, 2.5GBASE-T1
    - BRIGHTLANE™ Q3244 (BGA package only)
      - Supported line rates: 10GBASE-T1, 5GBASE-T1, 2.5GBASE-T1
  - Multi-speed SerDes supports 2500BASE-X, 5G-USXGMII, 10G-USXGMII, 5GBASE-R, XFI system interfaces
  - MDC/MDIO and SPI management interface
  - IEEE 802.1AS, 802.1AS-REV–Precision Timing and Synchronization for Time-Sensitive Applications
  - IEEE 1588 Precision Clock Synchronization Protocol
  - IEEE 802.1AE-2018 MACsec with 128/256-bit AEC encryption
  - IEEE 802.3br-2016 Preemption
  - Automatic polarity detection and correction on MDI pair.
  - Integrated filter network for reduced BOM cost and board space
  - Integrated temperature sensor
  - OPEN Alliance TC10 Sleep/Wake
  - Software programmable LED modes
  - Advanced VCT for cable diagnostics
- Compliance
  - AECQ-100

- Automotive Grade 2 operation: -40 °C to +105 °C ambient operating temperature range

- Packages
  - BRIGHTLANE™ Q3241/Q3242/Q3244 devices
    - 104-pin LFBGA, 7.0 mm ×11.0 mm, 0.8 mm pitch
  - BRIGHTLANE™ Q3241 device
    - 48-Pin QFN, 7.0 mm ×7.0 mm, 0.500 mm pitch

Applications

- Automotive infotainment systems
- Advanced driver assistant systems
- Inter-zone connectivity
- Telematics Control Systems

Table 1: BRIGHTLANE™ Q3241/Q3242/Q3244 Device Features

		104-pin LFBGA Package			48-pin QFN Package
Line Interface	**System Interface**	**BRIGHTLANE™ Q3241**	**BRIGHTLANE™ Q3242**	**BRIGHTLANE™ Q3244**	**BRIGHTLANE™ Q3241**
2.5GBASE-T1	2500BASE-X (Clause 36)	Yes	Yes	Yes	Yes
	10G/5G USXGMII	Yes	Yes	Yes	Yes
5GBASE-T1	5GBASE-R (Clause 129)	No	Yes	Yes	No
	10G/5G USXGMII	No	Yes	Yes	No
10GBASE-T1	10GBASE-R (Clause 49)/XFI	No	No	Yes	No
	10G USXGMII Auto-Negotiation based on Clause 37	No	No	Yes	No

Figure 1: BRIGHTLANE™ Q3241/Q3242/Q3244 BGA Device Block Diagram

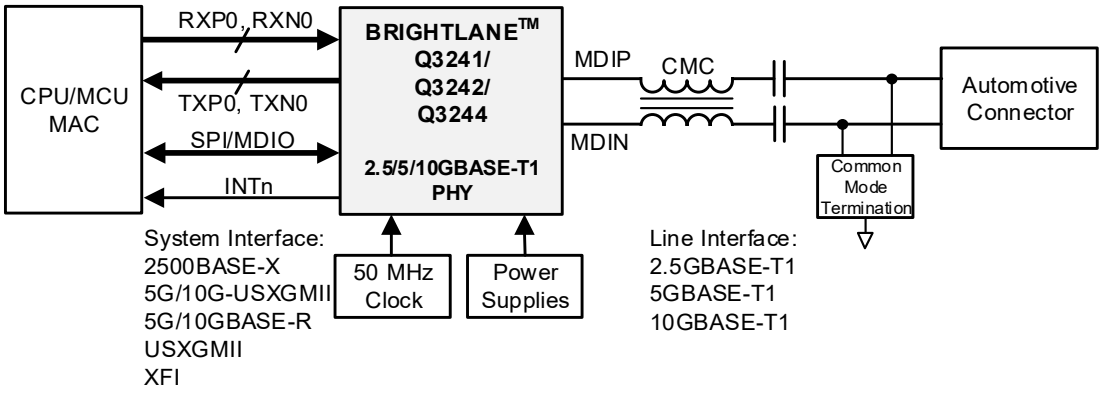


Figure 2: BRIGHTLANE™ Q3241 QFN Device Block Diagram

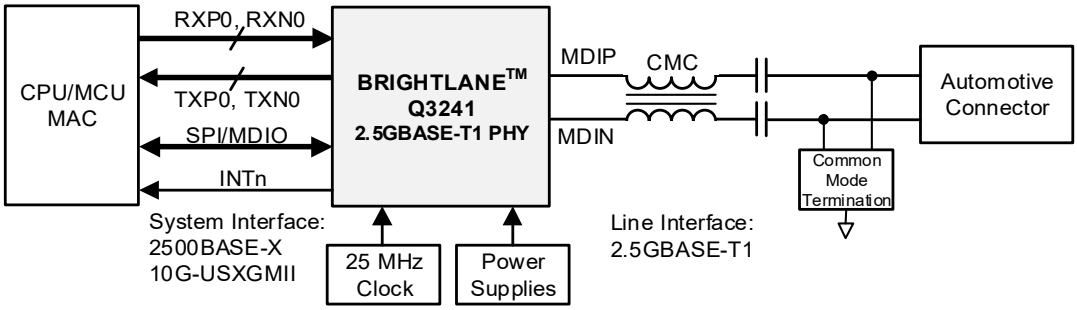


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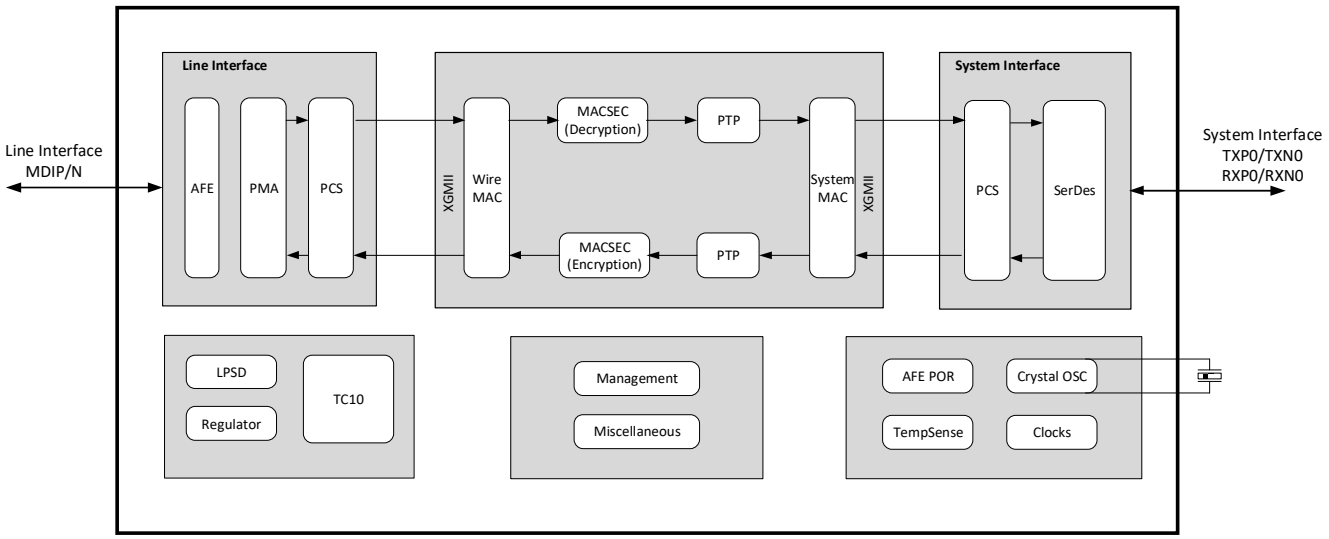
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1 Functional Descriptions

The device is an Ethernet transceiver with supported speeds of 2.5GBASE-T1 (QFN) or 2.5G/5G/10GBASE-T1 (BGA). Figure 3 shows the functional blocks of the device.

Figure 3: Functional Block Diagram



1.1 Copper Media Dependent Interface (MDI)

The line interface consists of the MDIP/N pins that connect to the physical media for 2.5G/5G/10GBASE-T1 mode of operation compliant to IEEE 802.3ch-2020 standard, including Clause 127 and Clause 36 interoperability.

1.1.1 Line Interface Features and Modes

- Integrates IEEE 802.3ch-2020 standard to support 2.5G, 5G and 10G Base-T1 speeds
  - Clause 45 MMD 1, MMD 3, and MMD 7 registers
- TC10/TC15
  - TC10 Port functionality as specified in OPEN Alliance Sleep Wake Specification for 2.5G/5G/10G rates
  - TC15 Advanced Cable Diagnostics

Transmit Side Line Interface

The device integrates MDI interface termination resistors as required in the IEEE 802.3 specification to prevent reflections. The resistors are designed to meet the strict IEEE and OPEN Alliance PSD and MDI return loss requirements.

The device incorporates a transmit AFE to generate filtered 4-level pulse amplitude modulation (PAM4) symbols.

Receive Side Line Interface

The device incorporates a receive AFE interface followed by a digital PMA on the receiver channel.

Degradation on the received signal can be caused by residual echo not removed by the hybrid and echo due to impedance mismatch, discontinuity, and variations in cable impedance along the cable. The device employs a fully developed digital echo canceller to adjust for echo impairments from the cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from the ADC output and uses a combination of feed-forward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise ratio (SNR).

The slave mode transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty resolving receive symbols due to unreliable synchronization; this results in higher bit error rates. In the device, an advanced digital phase-locked loop is used to recover and track the clock timing information from the receive signal.

1.1.2 IEEE Power Down Mode

The standard IEEE power down mode is entered by register control. The PHY does not respond to any system interface signals except the serial management interface (SMI). It also does not respond to any activity on the copper media. In this power down mode, the PHY cannot wake up on its own by detecting activity on the media.

1.1.3 Automatic Polarity Detection and Correction

The device has the capability to automatically detect and correct the polarity on the receive side when a polarity swap is observed.

1.2 System Interface

1.2.1 System Interface Features and Modes

The BGA package supports various SERDES based system interfaces: 2.5G/2500BASE-X, 5G-USXGMII, 10G-USXGMII, 5GBASE-R, and XFI.

The QFN package supports SERDES based system interfaces: 2500BASE-X and 10GUSXGMII.

The System Interface features are as follows:

- 802.3 PCS Protocol Features
- 2500BASE-X (Clause 36)
- 5G USXGMII (2.5/5G wire speeds)
- 10G USXGMII (2.5/5/10G wire speeds)
- 10GBASE-R (Clause 49)
- 5GBASE-R (Clause 129)
- USXGMII Auto-Negotiation based on Clause 37

The SerDes modes can be configured as shown in Table 2.

Table 2: Modes

Mode	Coding	SerDes	Line Rate
2500BASE-X	8B/10B	3.125G	2.5G
5GBASE-R	64B/66B	5.15625G	5G
5G-USXGMII	64B/66B	5.15625G	2.5G/5G
10G-USXGMII	64B/66B	10.3125G	2.5G/5G/10G
XFI	64B/66B	10.3125G	10G

2500BASE-X leverages 8b/10b encoding as specified in the IEEE802.3 Clause 36 specification using a standard GMII configuration. XGMII to GMII converter is used to support 2500Base-X.

2.5/5/10G USXGMII and 10G BASE-R utilize 64/66 bit encode/decode as specified in the IEEE802.3 Clause 49 and use a standard XGMII interface.

Short Preamble FIFO and Minimum IPG

Short Preamble up to 2B can be corrected. The minimum IPG to be maintained after short preamble correction can be maintained. A FIFO overflow condition can happen if there is not enough IPG to delete for adding preamble. For example, if 12B IPG needs to be maintained and 2B correction is needed. FIFO will overflow for such cases since there is not enough IPG.

Table 3: IPG Requirements

PCS Mode	Minimum IPG in Bytes from MAC
2500BASE-X	8
5/10GBASE-R	5
2.5/5/10G-USXGMII	8

The device is designed for ±100PPM, which surpasses the IEEE specification of ±50PPM. The maximum packet size that can be support is 10KB.

2500BASE-X False Carrier Errors

The device does not convert false carrier character received to Errors on XGMII interface. It converts false carrier symbols to Idles on the XGMII interface.

1.2.2 SerDes PCS Modes

The PCS Modes are noted in Table 4: PCS Modes.

Table 4: PCS Modes

CFG_MODE	PCS_MODE	SerDes SPEED (Gbps)
001	2500BASE-X	3.125
100	5GBASE-R	5.15625
101	10GBASE-R	10.3125
110	5G USXGMII	5.15625
111	10G USXGMII	10.3125

1.2.3 SerDes PCS Unit

2500BASE-X PCS Implementation

For 2500BASE-X mode, speed is fixed at 2500 Mbps. Transmit and receive data paths leverage the 1000BASE-X 8B/10B protocol as defined in the IEEE802.3z clause 36 specification.

TX path of 2500Base-X is as shown in the figure below. Standard GMII interface is used to transmit data. GMII <-> XGMII converters are not shown in the below diagrams since they define how 2500BASE-X is implemented inside the PCS module.

10GBASE-R Implementation

10GBASE-R is implemented as per IEEE 802.3-2018 clause 49. This PCS can connect directly to one of the 10GBASE-R Physical Layers: 10GBASE-SR, 10GBASE-LR, 10GBASE-ER, 10GBASE-LRM, and 10GBASE-KR.

The 10GBASE-R is based on a 64B/66B code. The 64B/66B code supports data and control characters, while maintaining robust error detection.

The following are the features of 10GBASE-R:

- Support the full-duplex Ethernet MAC.
- Provide 10 Gbps data rate at the XGMII.
- Allow for a nominal network extent of up to 40 km.
- Support a BER objective of 10^{-12}.

The PCS service interface is the 10 Gigabit Media Independent Interface (XGMII), which is defined in ieee 802.3 Clause 46. The XGMII provides a uniform interface to the Reconciliation Sublayer for all 10 Gb/s PHY implementations (e.g., not only 10GBASE-R but also other types of 10 Gigabit PHY entities).

The 10GBASE-R PCS provides all services required by the XGMII, including the following:

a. Encoding (decoding) of eight XGMII data octets to (from) 66-bit blocks (64B/66B).

b. Transferring encoded data to (from) the PMA in 16 bit transfers.

c. Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use.

5000/5GBASE-R Implementation

The 5GBASE-R PCS is identical to the 10GBASE-R PCS specified in Clause 49 with the exception that it is running at one half the data rate.

1.2.4 SerDes USXGMII

USXGMII is an architecture that allows for the definition of specific interfaces in a way that maximizes reuse and reduces risk. USXGMII isn't a single protocol, but rather an architecture that allows for the definition of specific interfaces in a way that maximizes reuse and reduces risk. For example, USXGMII can be used to NGBASE-T (2.5G/5G) and 10Gbps ASIC to/from Copper PHY interface. To connect with MAC, with a link speed of 2.5/5/10Gbps, XGMII interface is used.

USXGMII leverages the 64B/66B PCS defined in IEEE 803.2ae Clause 49. The PCS is unchanged with additional functionality being added via the "ordered set" mechanism defined by IEEE.

USXGMII Features

- System Interface operates in full-duplex mode only
- Ability to send PTP time stamp from PHY to MAC to improve accuracy/jitter on encrypted/non-encrypted PTP packet with MACSec is in the ASIC
- Hardware assisted auto-negotiation for all supported speeds
- Flexibility to add new features using Extension Field in the pre-amble

USXGMII uses two data signals in each direction to convey frame data and link rate information between a single or multi-port PHY and the Ethernet MAC(s).

Table 5: USXGMII Single Port Options

MAC-PHY Type	Network Types	Replications Lowest to Highest data speed	PCS	SerDes Speed in Gbps
10G-USXGMII	2.5/5/10G	4, 2, 1	Clause 49	10.3125
5G-USXGMII	2.5G/5G	2, 1	Clause 49	5.15625

1.2.5 System Interface Registers

The System interface has register maps for 16-bit register space. Registers that are wider than 16 bits must be access by multiple 16 bit register transactions.

Table 6: System Interface MDIO Registers

LSB	MSB	Name	Description
0x8000	0x8FFF	XGKR IEEE	This address space contain the standard IEEE registers for Base-R/USXGMII modes
0x9000	0x9FFF	XGKR Vendor Defined	This address space contain the vendor defined for Base-R/USXGMII modes
0xA000	0xAFFF	GKX IEEE	This address space contain the standard IEEE registers for 2500 Base-X modes
0xB000	0xBFFF	GKX GEN	This address space contain the vendor defined for 2500 Base-X modes
0xD000	0xD7FF	Ingress PPM FIFO	Contains the registers of Ingress PPM FIFO module
0xD800	0xDFFF	Egress PPM FIFO	Contains the registers of Ingress PPM FIFO module
0xF000	0xF8FF	COMMON VENDOR	Contains common vendor registers such as test, loopback and internal controls for logic debug
0xF900	0xF9FF	XGMII STATS	Counters at the Rx/TX and RX/TX PPM FIFO XGMII-interfaces of the of the Datapath. Counters are implemented as external from a SystemRDL perspective and are part of a lib_counter_block design_lib. This library module allows for more advanced constructs such as setting how counters shall be cleared. Counters are 48 bit.
0xFB00	0xFB40	Interrupts	Contains Interrupt Mask/Map/Status registers
0xFC00	0xFFFF	Common	Contains Common registers for PCS settings

USXGMII Auto-Negotiation and MDIO Auto-Negotiation Control

USXGMII Auto-neg mechanism is based on Clause 37 (Figure 37-6) plus additional management control to select USXGMII mode. The PHY must provide a USXGMII enable control configuration via MDIO.

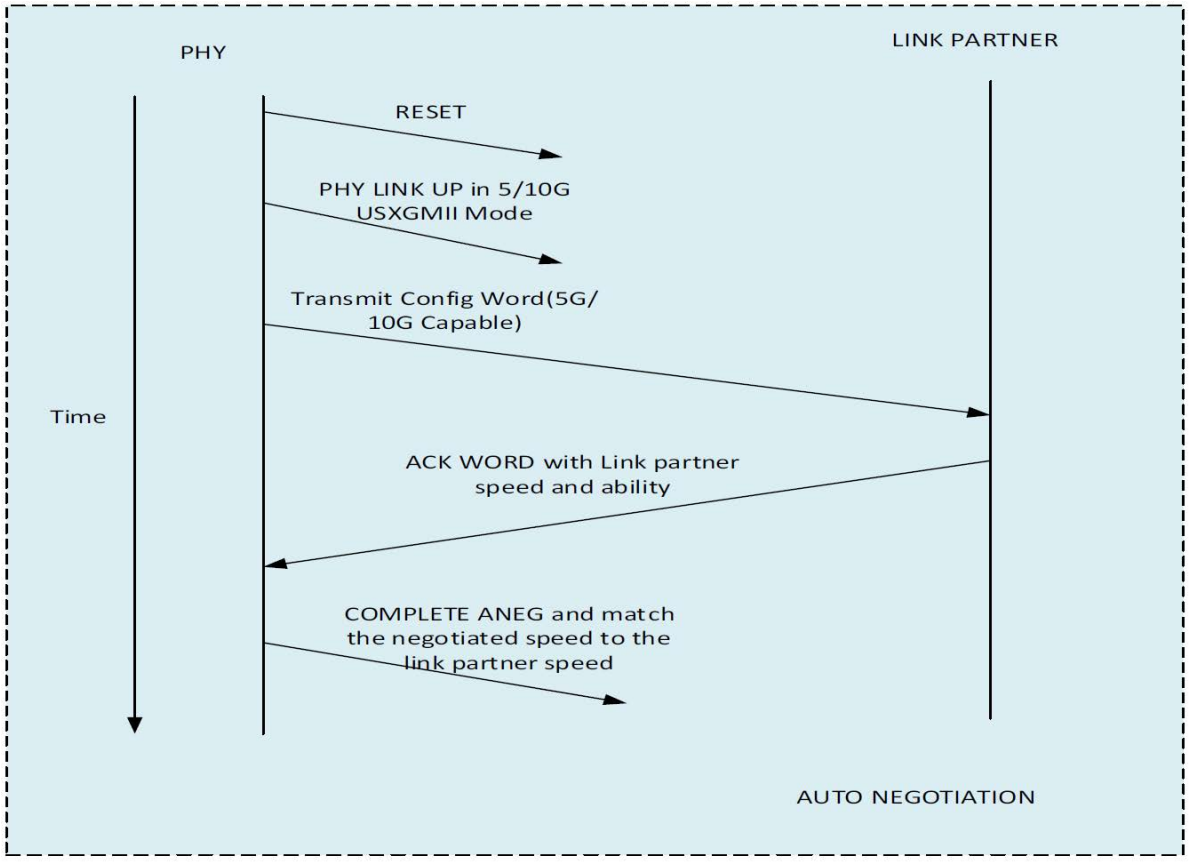
On power reset, USXGMII enable bit is de-asserted (logic “0”) and system interface on Port ASIC and PHY must assume normal XGMII/XFI (Clause 46/49) operation for 10Gbps. Once USXGMII enable bit is enabled via MDIO, auto-neg operation should follow Clause 37-6 functions with following modifications.

At the XGMII interface, Auto-neg message uses the format below:

Table 7: XGMII Auto-Neg Message Format

TXC[3:0]	TXD[31:24]	TXD[23:16]	TXD[15:8]	TXD[7:0]
1	Character Control 0x9C	AN_WORD[15:8]	AN_WORD[7:0]	Opcode for auto-neg = 0x03 (Cisco Spec)

Figure 4: Auto-Negotiation Process



1.2.6 System Interface PRBS Testing

The device supports the following PRBS test sequences:

PRBS_1T

PRBS_2T

PRBS_4T

PRBS_5T

PRBS_8T

PRBS_10T

PRBS7

PRBS9

PRBS11: F(X) = X^11 + X^9 + 1

PRBS11_0 : F(X) = X^11 + X^10 + X^6 + X^5 + 1

PRBS11_1 : F(X) = X^11 + X^9 + X^6 + X^5 + 1

PRBS11_2 : F(X) = X^11 + X^8 + X^6 + X^4 + 1

PRBS11_3 : F(X) = X^11 + X^7 + X^6 + X^4 + 1

PRBS15

PRBS16

PRBS23

PRBS31

PRBS32

NOTE: For PRBS_xT, x is the number of ‘1’s’ followed by the same number of ‘0’s’ of the generated pattern. For example: PRBS_4T means 11110000111100001111000011110000….

1.2.7 XGMII Statistics

The device supports 48-bit counter statistics on XGMII TX/RX interfaces. It tracks the following statistics.

- Egress frames (48-bit)
- Ingress frames (48-bit)
- CRC/FCS errors (48-bit)

1.3 Resets

1.3.1 Hardware Reset

The device is forced into Reset mode when pin RESETn is held LOW. provided all voltage supplies are above the undervoltage threshold. Refer to Table 31: Reset Timing on page 48 for Reset Timing details.

All register bits are reset to their default values in Reset mode and hardware configuration are sampled at deassertion of the reset signal.

1.3.2 Software Reset

Software reset can be issued via registers to clear the datapath and re-establish link on both the System Interface and Copper Interface. Hardware configuration is maintained.

1.4 Undervoltage (UV) Detection

When enabled by register writes, the device monitors the status of the supply voltages continuously. Once any of the following supply voltages, DVDD, AVDD08, AVDD12, AVDD33, or VDDIO drops below the specified minimum operating level, the device transitions to Standby/Fail-safe mode automatically. The device will remain in Fail-safe mode until the host issues a reset. If Undervoltage (UV) detection is enable, a UV Recovery interrupt is generated, and corresponding bit is set in Interrupt Status register.

1.5 Temperature Sensor

The device features an internal temperature sensor that can be used to read the internal die temperature and also can be used to trigger over temperature interrupts if the die temperature exceeds a fixed threshold.

1.6 Interrupts

The device contains an interrupt structure that can indicate both functional interrupt, fatal interrupts, and non-fatal interrupts. The external interrupt pin is used to indicate an interrupt to host using the device pin INTn. The INTn pin is active low, an interrupt is indicated by driving 0.

Fatal events such as uncorrectable memory errors, clock failure, or boot failure are non-maskable interrupts.

During the Host Configuration time, additional interrupts such as the link change interrupt, CPU watchdog interrupt, and uncorrectable memory error interrupts can be configured after link up.

1.7 Power Supplies and Management

The device requires a 3.3V, 1.2V and 0.84V supply for the operation. The digital I/Os can operate at 1.8V, 2.5V or 3.3V set at VDDIO supply.

Note

- If VDDIO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.
- The XTAL_IN pin is powered by AVDD12 (1.2V) and is not 2.5V/3.3V tolerant.

1.7.1 Low Power Modes

Two low power modes are supported in the device:

- IEEE Power Down mode
- OPEN Alliance TC10 Sleep Mode

1.7.1.1 IEEE Power Down Mode

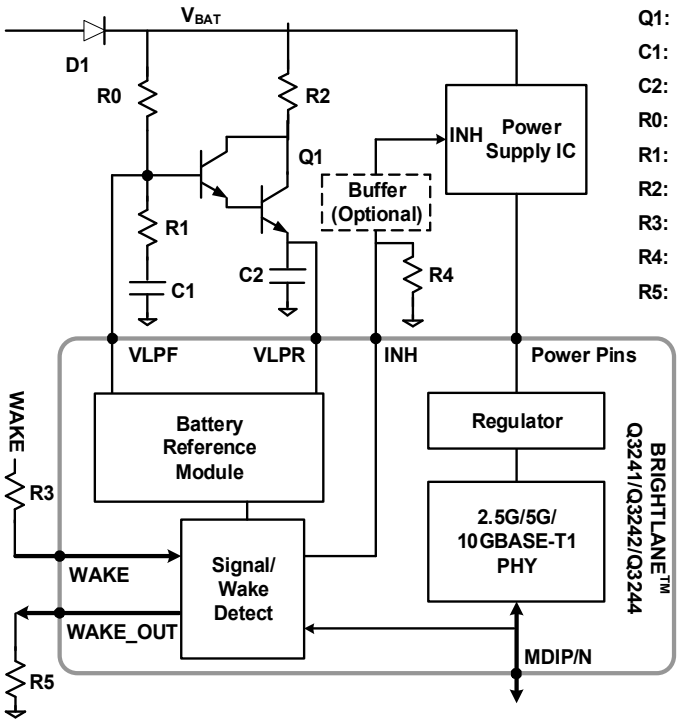
The standard IEEE power down mode is entered by setting registers. In this mode, the PHY does not respond to any system interface signals except the MDC_SPI_CLK/MDIO_SPI_MOSI. It also does not respond to any activity on the copper media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media.

1.7.1.2 Open Alliance TC10 Sleep Mode

The device can operate in a low power sleep mode with minimal standby current from the battery voltage with the main supply shut off. During this mode, the device can continuously monitor the WAKE pin, and respond to wake-up pulse command as specified in OPEN Alliance Sleep/Wake-up Specification. Figure 5 shows the Low Power Signal Detect (LPSD) schematic.

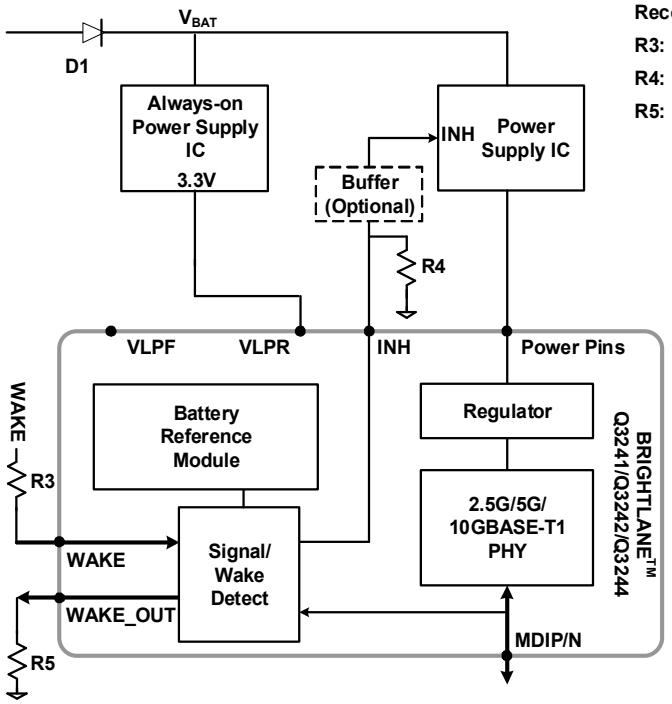
Figure 5: Low Power Signal Detect (LPSD) Block Diagram - Option 1



Recommended components:

Q1:	BCV47 (NPN)
C1:	2.7 nF
C2:	2.2 uF
R0:	2 Mohm
R1:	100 kohm
R2:	200 ohm
R3:	25 kohm (not needed if WAKE VIH ≤ 3.3V)
R4:	10 kohm
R5:	10 kohm

Figure 6: Low Power Signal Detect (LPSD) Block Diagram - Option 2



Recommended components:

R3:	25 kohm (not needed if WAKE VIH ≤ 3.3V)
R4:	10 kohm
R5:	10 kohm

For LPSD electrical details, refer to Section 4.5, Low Power Signal Detect (LPSD) Electrical Specifications, on page 62.

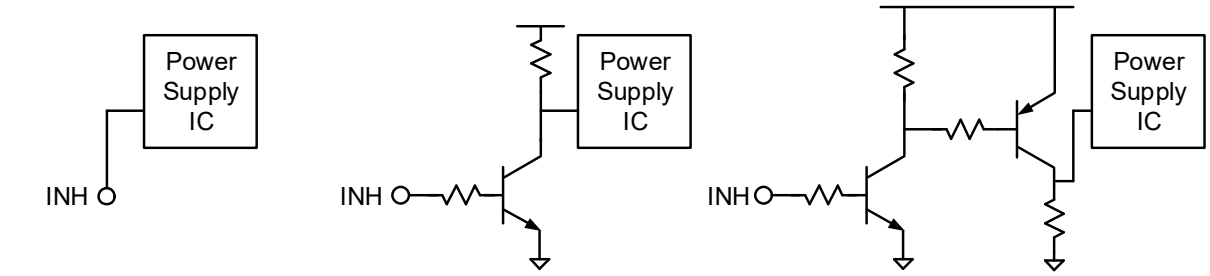
LPSD Application Notes

- WAKE bus voltage:
  - **a.** If WAKE bus is running less than or equal to 3.3V supply, the WAKE bus can be directly connected to the WAKE pin.
  - **b.** If WAKE bus is running on battery supply, external series 25 kΩ resistor is required to drive the WAKE pin.
- INH output:

Power supply IC EN/INH pin can be driven by BRIGHTLANE™ Q3244 INH pin in typical cases. For higher voltage and current requirements, external buffer may be added.

- **a.** If Power Supply IC EN input VIH < 1.4V and load current < 50 µA, INH pin can directly connect to Power Supply IC.
- **b.** Otherwise, external buffer components are required.
- **c.** For example configurations, see Figure 7.
- **d.** INH output needs to control EN input of all power supply ICs that power the device.

Figure 7: INH Output Example Configurations



Active (power on) High – Output high level at 1.4V – 1.9V @ < 50 µA load

Active (power on) Low

Active (power on) High

- Wake-up application scenarios – four cases of wake-up schemes can be supported:
  - Case 1: Local wake-up and remote wake-up.
    - WAKE from host controller. 3.3V or VBAT level can be accepted.
    - For VLPR, VLPF, and INH, see Figure 5.
  - Case 2: No local wake-up. Remote wake-up support.
    - WAKE = VSS. For VLPR, VLPF, and INH, see Figure 5.
    - Or use case 1 configuration but use registers to program.
  - Case 3: Local wake-up only. No remote wake-up.
    - Use case 1 configuration. Use register program to disable remote wake-up.
  - Case 4: No local wake-up. No remote wake-up.
    - WAKE = VSS or NC. VLPR = 3.3V, VLPF, and INH = NC.

1.7.1.3 Sleep/Wake-up

As an IEEE and OPEN Alliance TC10 compliant 2.5G/5G/10GBase-T1 Ethernet PHY, the device supports Wake-up Pulse (WUP), Wake-up Request (WUR) and Low Power Sleep (LPS) commands.

1.7.1.4 Wake-up

The PHY can be woken up by a local wake-up pin, a wake-up request command or a wake-up pulse from link partner. Upon detection, a wake-up interrupt is generated, and the wake-up source is flagged in the Wake-up Status Register. The source bits are cleared when device is in reset mode.

Local Wake-up

In Sleep Request and Sleep modes, a positive pulse on the WAKE pin meets minimum duration time ($T_{WAKE,PW}$) triggers a local wake-up.

Low Power Sleep (LPS) and Wake-Up Request (WUR)

The Low Power Sleep (LPS) and Wake-Up Request (WUR) is defined in Section 8.1 of OPEN Sleep/Wake-Up Specification. An LPS and WUR command is transmitted through transmitting a single OAM frame with the respective bit set.

1.7.1.5 Wake-Up Pulse

The Wake-Up pulse (WUP) is defined in Section 8.2 of OPEN Sleep/Wake-Up Specification. A WUP command is a special wake up pattern transmitted over MDI for remote wake up.

1.7.2 Power Supply Sequencing

The external power supply rails can ramp up in any order within 20 ms from first rail to last rail delay with one requirement: DVDD and AVDD08 rails must be sourced from the same power supply so that they are ramped up/down together. After all supplies are up and stable, and with a minimum of 1 ms of RESETn assertion, the device can enter normal operation upon the de-assertion of RESETn.

Additionally, each individual rail must ramp up monotonically from 10% to 90% of nominal voltage within 5ms when TC10 is used.

The removal of power supply rails can be in any order (with the same requirement that the DVDD and AVDD08 rails ramp down at the same time). All power supply rails must be removed and reached voltage levels <10% of nominal voltage (i.e., inactive state) before a new power up event starts.

Caution

DVDD and AVDD08 must use the same 0.84V supply source.

1.7.3 Status of Functional Block in Each Mode

Table 8: Status of Functional Block in Each Mode

Functional Block Pin(s)	Reset	Fail-safe	Normal Operation	OPEN Alliance Sleep	IEEE Power Down
MDI	Disable	Disable	Functional	Functional[1]	Disable
SerDes	Off	Off	On	Off	On
REFCLK/Crystal	Reset	On	On	Off	On
RESETn	Functional	Functional	Functional	Disable	Functional
MDC_SPI_CLK/ MDIO_SPI_MOSI	Disable	Functional	Functional	Disable	Functional
WAKE	Disable	Disable	Functional	Functional	Functional
INH	Functional	Functional	Functional	Functional	Functional
INTn	De-asserted	Functional	Functional	Disable	Functional

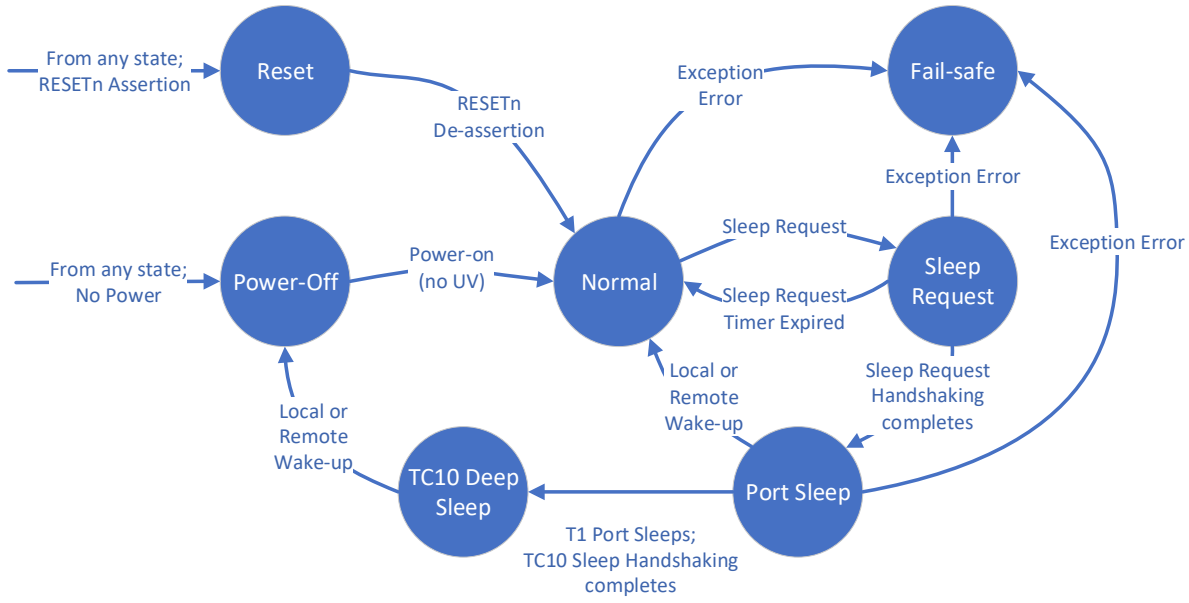
1. Only remote wake-up function is available.

1.7.4 Transitions of Each Mode

Figure 8 shows the device mode transition diagram. The following event, listed by priority, trigger the transitions.

- Power On/Off
- Hardware RESETn
- Undervoltage (UV)
- Management Command:
  - Local and remote Sleep/Wake-up commands

Figure 8: Transitions in each mode



1.8 Device Configuration

The device can be configured in two ways:

- Hardware configuration strap options (unmanaged applications)
- Register writes via MDC/MDIO or SPI interfaces (managed applications)

The Master/Slave configuration bits can be overwritten by software. PHYAD modes cannot be overwritten.

1.8.1 Hardware Configuration

Hardware CONFIG pins carry multiple levels of information on a single pin, and configuration is achieved by connecting each CONFIG[4:0] pin as noted in Table 9:

Table 9: CONFIG[4:0] Configuration Values

CONFIGx Connected to	Configuration Value
Pull-up to VDDO	0
Pull-down to VSS	1
CONFIG_OUT0	2
CONFIG_OUT1	3

Table 10: Configuration for Firmware Boot Source, MDIO vs. SPI Mode

CONFIG0 Value	BootLoad Firmware	SMI Interface
0	ROM	MDIO Mgmt
1	ROM	SPI Mgmt
2[1]	Flash[2]	MDIO Mgmt
3[1]	Flash[2]	SPI Mgmt

1. CONFIG 0 Value = 2 and 3 not applicable to QFN Package
2. Flash only supported for Rev A1 silicon (prototyping)

1.8.1.1 PHYAD (PHY Address)

The address of the PHY is determined from hardware configuration of CONFIG2 and CONFIG1 pins.

The PHY address is four bits, which allows for 16 unique PHY Addresses that can be accessed from a MDIO bus.

Table 11: PHYAD Configuration

CONFIG2 Value	CONFIG1 Value	.PHYAD[3:0]
0	0	4’d0
	1	4’d1
	2	4’d2
	3	4’d3
1	0	4’d4
	1	4’d5
	2	4’d6
	3	4’d7
2	0	4’d8
	1	4’d9
	2	4’d10
	3	4’d11
3	0	4’d12
	1	4’d13
	2	4’d14
	3	4’d15

Mode Configuration is achieved by connecting CONFIG[4:3] as noted in Table 12.

5000BASE-R shall only be enabled via SMI control in the desired application as pin encodings are used for most common customer configurations. Additionally, since the 5GBASE-T1/10G USXGMII are not typical modes, these modes shall also only be explicitly enabled through SMI control.

Table 12: Mode Configuration

CONFIG4 Value	CONFIG3 Value	Line CONFIG	SYSTEM CONFIG	MASTER/SLAVE
0	0	10GBASE-T1	10GBASE-R	MASTER
	1	10GBASE-T1	10G USXGMII	MASTER
	2	5GBASE-T1	5GBASE-R	MASTER
	3	5GBASE-T1	5G USXGMII	MASTER
1	0	Reserved	Reserved	Reserved
	1	2.5GBASE-T1	2500BASE-X	MASTER
	2	2.5GBASE-T1	10G USXGII	MASTER
	3	2.5GBASE-T1	5G USXGMII	MASTER
2	0	10GBASE-T1	10GBASE-R	SLAVE
	1	10GBASE-T1	10G USXGMII	SLAVE
	2	5GBASE-T1	5GBASE-R	SLAVE
	3	5GBASE-T1	5G USXGMII	SLAVE
3	0	Chip Isolate (Copper and System Link Disable)		
	1	2.5GBASE-T1	2500BASE-X	SLAVE
	2	2.5GBASE-T1	10G USXGMII	SLAVE
	3	2.5GBASE-T1	5G USXGMII	SLAVE

1.9 Diagnostics

1.9.1 Packet Generator and Packet Checker

1.9.1.1 CRC Error Counter and Frame Counter

The cyclic redundancy check (CRC) counter and packet counters are available in the device. The error counter and packet counter features are enabled through register writes, and each counter is stored in sixteen register bits. The CRC error and packet counters do not distinguish between IEEE 802.3br express and preemptable packet.

1.9.1.2 Packet Generator

The device contains a packet generator.

The packet generator supports fixed length packets of 64 or 1518 bytes (including CRC) that can be transmitted out via the Copper interface, separated by 12 bytes of inter-packet gap (IPG). The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5 pattern, a pseudo random pattern, or a constant payload of 0 or 1. A correct CRC is appended to the end of the packet. An error packet can also be generated.

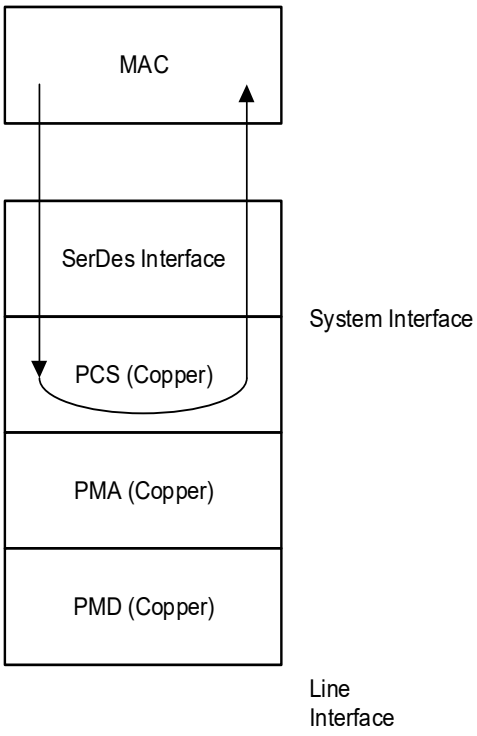
1.9.2 Loopbacks

The device implements various loopback paths.

1.9.2.1 System Interface Loopback

The functionality, timing, and signal integrity of the system interface can be tested by placing the device in system interface loopback mode. In this loopback mode, the data received from the MAC is not transmitted out on the copper interface. Instead, the data is looped back and sent to the MAC. During loopback, copper link will be lost, and packets will not be received.

Figure 9: MAC Interface Loopback Diagram - Copper Media Interface

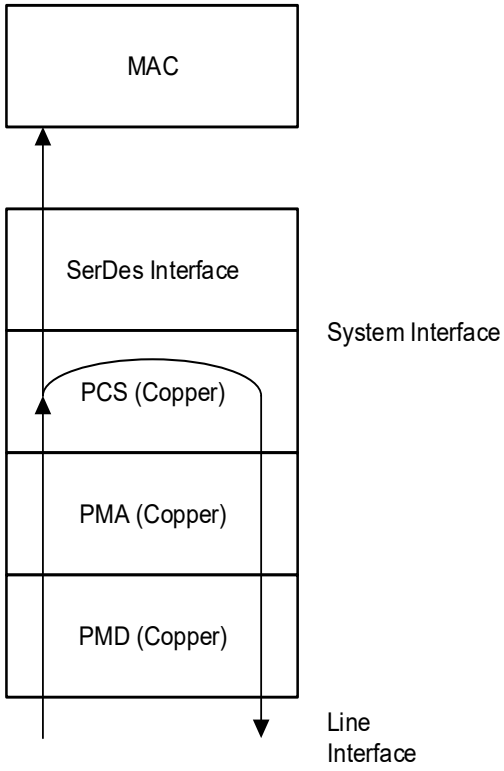


1.9.2.2 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner received by the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. Once link is established, the line loopback mode can be enabled.

Figure 10: Copper Line Loopback Data Path



1.9.3 Advanced PHY Diagnostic Features

The device supports advanced diagnostic features as specified in “Advanced Diagnostic Features for automotive Ethernet PHYs” by OPEN Alliance.

Table 13: Supported Advanced PHY Diagnostic Features

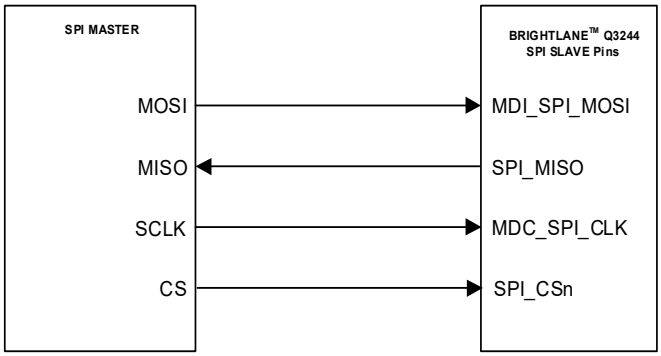
Group	Group Name	Parameter	Parameter Name	Description	Support
DCQ	Dynamic Channel	SNR	SNR Operating Margin	The SNR Operating Margin value of the symbol detection in accordance to IEEE specification	Yes
HDD	Harness defect detection	OS	OPEN/SHORT detection	Cable-Harness errors (short circuit or open line) shall be detected	OPEN of one bus wire
					OPEN of both bus wires
					SHORT between both bus wires
					SHORT of both bus wires to VBAT or GND
--	TDR based cable	TDR	SHORT/OPEN/ DISTANCE	Cable harness error detected by TDR-like approach	Yes
LQ	LinkQuality	LTT	Link-training time	The time of the last link training shall be stored	Yes
		LRT	Local Receiver Time	The timing of the local receiver shall be stored	Yes
		RRT	Remote Receiver Time	The timing of the remote receiver shall be stored	Yes
		LFL	Link Failures and Losses	Number of link losses since the last power cycle shall be stored	Yes
		COM	Communication Ready	Optimized Link Status information. Signals when communication is possible	Yes
POL	Polarity detection/ correction	DET	Polarity detect	According to the IEEE specifications of 2.5G/5G/10GBASE-T1	Yes
		COR	Polarity correct	According to the IEEE specifications of 2.5G/5G/10GBASE-T1	Yes
FEC	Forward Error Correction	REC	Receive Error Counter	RS-FEC Receive Error Counter	Yes

1.10 Controls and Status

1.10.1 SPI Slave Interface

The device has one SPI interface, which operates in SPI Slave mode. The SPI Slave interface is one of the device's management interfaces that can be used to access the device registers. It supports Mode 0 and Mode 3 operation based on Motorola SPI Block Guide, supporting two register access protocols: 32-bit address with 32-bit data or 16-bit data.

Figure 11: SPI Slave Interface Block Diagram



1.10.2 Link Disconnect Counter

The link disconnect counter increments every time the link transitions from up to down. Link Drop Counter is a R/W register that needs to be cleared by setting it to 0.

1.11 Precision Time Protocol (PTP) Time Stamping Support

Precision Timing Protocol (PTP) is used by IEEE specifications to determine the time of day for systems across a network. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to time stamp the PTP frames with high precision as close to the physical wires as possible. As such, doing the time stamping in the PHY increases the accuracy compared to doing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

The time stamping core supports time stamping of frame formats as defined in IEEE 802.1AS, IEEE 802.1AS-REV, IEEE 1588-2002 (v1), and IEEE 1588-2008 (v2) frames.

1.12 MACsec Support

1.12.1 General Features

IEEE 802.1AE Media Access Control Security (MACsec) is an industry standard security technology that provides secure communication for layer 2 Ethernet traffic. The device supports wire-speed Ethernet MACsec protocol. It is a highly scalable and cost-effective encryption solutions to address the data security issues in Automotive applications. Combining Infineon's strength in high speed, high performance mixed-signal I/O and industry leading CMOS silicon technology, the PHY products provide line-rate encryption and authentication in addition to the connectivity among Ethernet ports.

The key features of MACsec function:

- Support IEEE 802.1AE-2018 with 128 and 256-bit encryption keys.
- Line rate of 2.5G/5G/10G for Multi-Gig operation.
- Number of secure association (SA) channels: 8
- Support both Authentication only and Authentication with Encryption modes.
- Support key change on each packet boundary.

1.13 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The device implements the instructions shown in Table 14. The instruction opcodes are shown in Table 14.

Table 14: TAP Controller Opcodes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
EXTEST_PULSE	00000101
EXTEST_TRAIN	00000110
BYPASS	11111111

The device reserves 5 pins called the Test Access Port (TAP) to provide test access: Test Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

1.13.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

1.13.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the device. Two functions are performed when this instruction is selected: sample and preload.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

The boundary scan register for P7_LED[1] is closest to TDO.

Table 15 lists the boundary scan order where:

Table 15: BRIGHTLANE™ Q324x Boundary Scan Chain

Pin	I/O
RXN0	observe_only
RXP0	observe_only
TXP0	Output enable
INTn	Input
INTn	Output
CONFIG3	Input
CONFIG3	Output
PTP_TRIG_IN	Input
PTP_TRIG_IN	Output
CONFIG4	Input
SLEEP_DIS	Input
SLEEP_DIS	Output
RESETn	Input
CONFIG2	Input
CONFIG0	Input
SPI_MISO	Input
SPI_MISO	Output
MDC_SPI_CLK	Input
MDD_SPI_MOSI	Input
MDD_SPI_MOSI	Output
XTAL	Input
XTAL_SEL	Input
LED	Input
LED	Output

1.13.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the to its external connections.

1.13.4 The CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path

between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

1.13.5 The HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

1.13.6 EXTEST_PULSE Instruction

The AC JTAG test modes can be selected for each port individually by scanning in the desired bit value into AC/DC select scan registers shown in the scan chain.

When the AC select is set, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the UOUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the UOUTP pins output the level specified by the test stimulus and UOUTN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the UOUTN pins output the level specified by the test stimulus and UOUTP pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the UOUTP pins again output the level specified by the test stimulus and UOUTN pins output the opposite level.

1.13.7 EXTEST_TRAIN Instruction

When the AC select is set, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the UOUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the UOUTP pins output the level specified by the test stimulus and UOUTN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the UOUTP/N will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the UOUTP pins again output the level specified by the test stimulus and UOUTN pins output the opposite level.

2 Signal Description

Table 16: Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
D	Open drain output
Z	Tri-state output
mA	DC sink capability
Ground	Ground to device
NC	No connect
RES	Reserved (Pull High) Reserved (Pull Low)

2.1 Device Pin Description

2.1.1 Line Interface

Table 17: Line Interface

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
F1 E1	17 16	MDIP MDIN	I/O	Bi-directional Differential Signals. Used for Data Transmit and Receive. Can operate in 10GBASE-T1, 5GBASE-T1, or 2.5GBASE-T1

2.1.2 System Interface

Table 18: System Interface

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
M1 L1	23 24	TXP0 TXN0	O	Differential Transmit Signals. Can operate in 2500BASE-X, 5G-USXGMII, 10G-USXGMII, 5GBASE-R, or XFI
N2 N3	25 26	RXP0 RXN0	I	Differential Receive Signals. Can operate in 2500BASE-X, 5G-USXGMII, 10G-USXGMII, 5GBASE-R, or XFI

2.1.3 Clock/Configuration/Management/PTP/Reset/IO

Table 19: Clock/Configuration/Management/PTP/Reset/IO

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
J1	21	XTAL_IN	I	Reference Clock Input. LFBGA Package - 50 MHz ± 50 ppm tolerance crystal reference. QFN package - 25 MHz ± ppm tolerance crystal reference Series resistors must be on XTAL_IN.
H1	20	XTAL_OUT	O	Reference Clock Output. LFBGA Package - 50 MHz ± 50 ppm tolerance crystal reference. QFN package - 25 MHz ± ppm tolerance crystal reference Series resistors must be on XTAL_OUT.
L8	41	CONFIG0	I	Global hardware configuration
K8	40	CONFIG1	I	
G8	43	CONFIG2	I	
C3	--	CONFIG3/ FLASH_SI	I	Dual-function Global hardware configuration and SPI Flash (Master) Interface.
C2	--	CONFIG4/ FLASH_SO	I	
A3	--	FLASH_CEN	O	SPI Flash Chip Select Output Connected to SPI Flash Chip Select if SPI Flash is used. If booting from ROM, connect to VDDIO using 10 kΩ resistor.
J7	36	MDC_SPI_CLK	I	Dual-function Management Interface Clock/SPI Slave Clock, Clock Input A continuous clock stream is not required when operating as MDC. If unused, this pin must be left floating
K7	35	MDIO_SPI_ MOSI	I/O	Dual-function Management Interface Data/SPI Slave Data Input. Requires a pull-up resistor with resistance between 1.5 kΩ and 10 kΩ.
J8	37	SPI_CSn	I	For BGA Package: SPI Slave Chip Select Input SPI_CSn can be used as GPIO in an alternative mode. If unused, it is recommended to connect this pin to VDDIO as no pull-up/down is configured by default. For QFN Package: Master/Slave Strap Option SPI_CSn is used as Master/Slave Strap option to configure the device: 0 = Slave 1 = Master

Table 19: Clock/Configuration/Management/PTP/Reset/IO (Continued)

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
H8	38	SPI_MISO/ CONFIG_OUT1	I/O	Dual-function SPI Slave Data Input/CONFIG_ OUT1 CONFIG_OUT1: Provides a value ‘3’ to be sampled by the CONFIG pins during a strap configuration.
B3	3	PTP_TRIG_IN/ FLASH_SCK	I	Dual-function PTP Trigger Event Request Input/SPI Flash Clock Output (SPI Master)
B4	4	PTP_TRIG_OUT	O	PTP Trigger Output
C7	45	RESETn	I	Hardware Reset, active-low. 0 = Reset 1 = Normal operation

2.1.4 JTAG

Table 20: JTAG/Test Pins

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
D7	47	TCK	I	JTAG Clock Input
E7	1	TDI	I	JTAG Data Input
M2	30	TDO	O	JTAG Data Output
C6	46	TRST_N	I	JTAG Reset This pin requires an external pull-up.
B7	44	TMS	I	JTAG Test Mode State
K4	33	TEST_SEL	I, PD	Test select. The TEST_SEL pin is used to place the chip into its manufacturing test modes. Do not connect this pin to anything other than VSS or improper device operation may result. 0 = Normal function mode 1 = Test Mode, JTAG pin used as JTAG interface The TEST_SEL pin is internally pulled low via a resistor so the pin should be left floating when unused.

2.1.5 High-Speed DAC (HSDAC) Test

Table 21: High Speed DAC (HSDAC) Test Pins

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
B1	--	HSDACN	Analog, O	Test pins. These pins are used to bring out a differential TX_TCLK.
C1	14	HSDACP		

2.1.6 Interrupt

Table 22: Interrupt

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
D4	5	INTn	O	Interrupt output. Does not support open-drain mode.

2.1.7 LED

Table 23: LED

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
K3	31	LED/ CONFIG_ OUT0	O	Dual-function LED/CONFIG_OUT0 CONFIG_OUT0: Provides a value ‘2’ for CONFIG pins to be sampled during strap configuration.

2.1.8 Reference

Table 24: Reference

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
A2	13	RSET	A	Constant Voltage Reference. An external 4.99 kΩ 1% resistor connection to VSS is required.

2.1.9 Power, Ground, and Internal Regulators

Table 25: Power and Ground

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
E3 G3 J3	15	AVDD08	Power	Analog Supply - 0.84V.
D2 G2	12 18 22	AVDD12	Power	Analog Supply - 1.2V. AVDD12 supplies additional analog macros/functionalities.
C4	19 27	AVDD33	Power	Analog Supply - 3.3V.
K2	--	AVDDLS	Power	Analog Supply - 1.2V.
E5 J6	2 32 42	VDDIO	Power	3.3V, 2.5V, or 1.8V Digital I/O Supply. VDDIO supplies all digital pins.
E4 F5 G4 H5	6 29 34 39 48	DVDD	Power	Digital Core Supply - 0.84V.

Table 25: Power and Ground (Continued)

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
A1 B2 D1 E2 F2 F3 G1 H2 H3 J2 K1 L2 N1 N4	--	AVSS	Ground	Analog ground.
A8 D5 F4 F6 G5 G7 H4 H6 H7 N8	--	VSS	Ground	Digital ground.
--	Epad	VSS	Ground	Ground to device. The 48-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.

2.1.10 Low Power Signal Detect (LPSD)

Table 26: Low Power Signal Detect

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
C5	9	INH	A, O	Output to control enable of the external regulator. This must be left floating when LPSD is not used.
A6	10	VLPR	A	If TC10 is enabled, VLPR is connected to an always-on power derived from battery. In other cases, VLPR needs to be connected to 3.3V supply rail.
A7	11	VLPF	A	Connect to external battery circuit. This must be left floating when LPSD is not used.
D3	8	WAKE	A, I	Local wake-up signals.
A5	7	WAKE_OUT	A, O	

2.1.11 Reserved and No Connect Pins

Table 27: Reserved and No Connect Pins

BRIGHTLANE™ Q324x BGA Pin #	BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Description
N6 N7	--	Reserved (Pull High)	RES	Reserved signal. **NOTE:** These pins must be pulled high to VDDIO.
A4 B5 B6 B8 C8 D6 D8 E6 E8 F7 F8 G6 J4 J5 K5 K6 L3 L4 L5 L6 L7 M3 M4 M5 M6 M7 M8 N5	28	No Connect	N/C	No-connect signal. These pins can be left unconnected.

2.2 Dual-function Pins

2.2.1 Dual-function Pins for BGA Package

Table 28: Dual-function Pins for BGA Package

BRIGHTLANE™ Q324x BGA Pin #	Pin Name	Pin Type	Primary Purpose	Alt1 Purpose	Alt2 Purpose
K3	LED/ CONFIG_ OUT0	O	CONFIG_OUT0/LED	GPIO (Input or Output)	--
H8	SPI_MISO/ CONFIG_OUT1	I/O	CONFIG_OUT1/ SPI Slave Data Out	--	--
J7	MDC_SPI_CLK	I	SPI Slave Clock	MDIO Clock	--
K7	MDIO_SPI_ MOSI	I/O	SPI Slave Data In	MDIO Data	--
J8	SPI_CSn	I/O	SPI Slave Chip Select	GPIO2	--
C2	CONFIG4/ FLASH_SO	I	CONFIG4	--	FLASH_SO
C3	CONFG3/ FLASH_SI	I/O	CONFIG3	--	FLASH_SI
G8	CONFIG2	I	CONFIG2	--	--
K8	CONFIG1	I	CONFIG1	--	--
L8	CONFIG0	I	CONFIG0	--	--
D4	INTn	O	System Interrupt	--	--
C7	RESETn	I	Chip Reset	--	--
B4	PTP_TRIG_OUT	O	GPIO	PTP_TRIG_OUT	--
B3	PTP_TRIG_IN/ FLASH_SCK	I/O	PTP_TRIG_IN	--	FLASH_SCK

2.2.2 Dual-function Pins for QFN Package

Table 29: Dual-function Pins for QFN Package

BRIGHTLANE™ Q3241 QFN Pin #	Pin Name	Pin Type	Primary Purpose	Alt1 Purpose	Alt2 Purpose
31	LED/ CONFIG_ OUT0	O	CONFIG_OUT0/LED	GPIO (Input or Output)	--
38	SPI_MISO/ CONFIG_OUT1	I/O	CONFIG_OUT1/ SPI Slave Data Out	--	--
36	MDC_SPI_CLK	I	SPI Slave Clock	MDIO Clock	--
35	MDIO_SPI_MOSI	I/O	SPI Slave Data In	MDIO Data	--
37	SPI_CSn	I/O	Mode Select: 0 = Slave 1 = Master		--
43	CONFIG2	I	CONFIG2	--	--
40	CONFIG1	I	CONFIG1	--	--
41	CONFIG0	I	CONFIG0	--	--
5	INTn	O	System Interrupt	--	--
45	RESETn	I	Chip Reset	--	--
4	PTP_TRIG_OUT	O	GPIO	PTP_TRIG_OUT	--
3	PTP_TRIG_IN/ FLASH_SCK	I/O	PTP_TRIG_IN	--	FLASH_SCK

2.3 104-Pin LFBGA and 48-Pin QFN Package Pinout and Pin List

The BRIGHTLANE™ Q3241/Q3242/Q3244 104-pin LFBGA and BRIGHTLANE™ Q3241 48-pin QFN pinout and pin list information are provided as an Excel file attachment. To open the attached Excel pin list file, double-click the pin icon below.

3 Timings

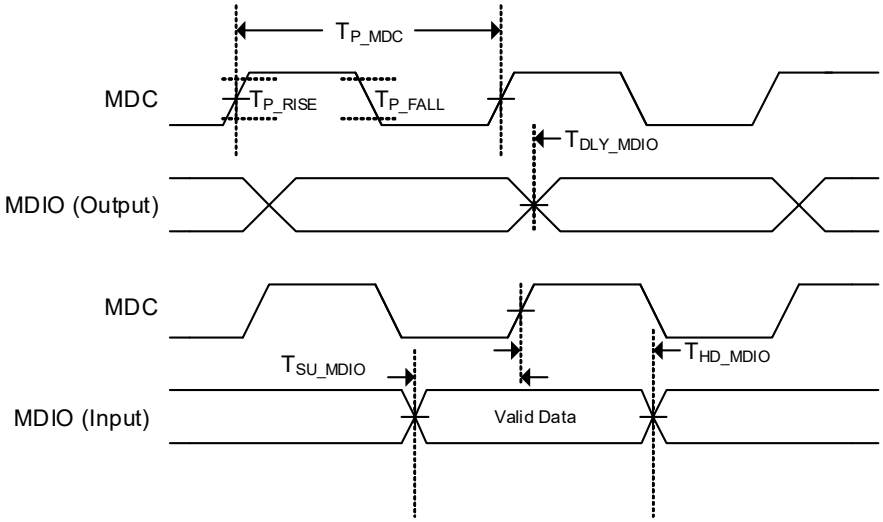
3.1 MDC/MDIO Timing

Table 30: MDC/MDIO Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)
Refer to Figure 12 for corresponding Symbol details.

Symbol	Parameter	Min	Typ	Max	Unit
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	0	–	31	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	10	–	–	ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	10	–	–	ns
T_{P_MDC}	MDC Period	80	–	–	ns[1]
T_{P_RISE}	MDC Rise Time	–	–	6	ns
T_{P_FALL}	MDC Fall Time	–	–	6	ns

1. Maximum frequency = 12.5 MHz.

Figure 12: MDC/MDIO Timing

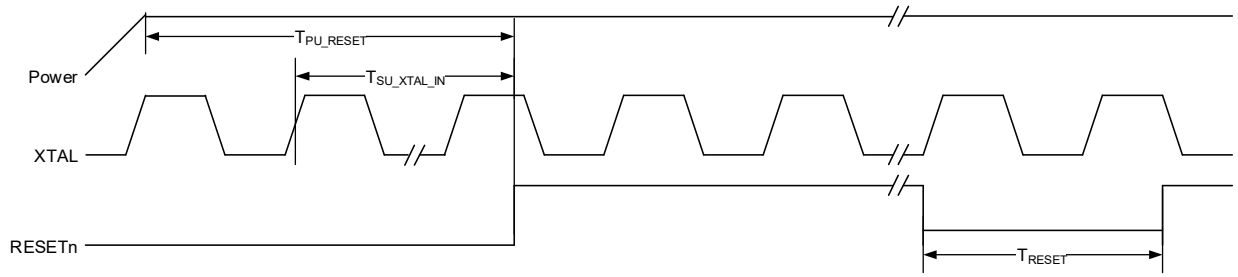


3.2 Reset Timing

Table 31: Reset Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)
Refer to Figure 13 for corresponding Symbol details.

Symbol	Parameter	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to RESETn de-asserted	1	–	–	ms
$T_{SU_XTAL_IN}$	Number of valid XTAL_IN cycles prior to RESETn de-asserted	10	–	–	period
T_{RESET}	Minimum reset pulse width during normal operation	1	–	–	ms
T_{RESET_MDIO}	Minimum wait time from RESET de-assertion to first MDIO access	1	–	–	ms

Figure 13: Reset Timing



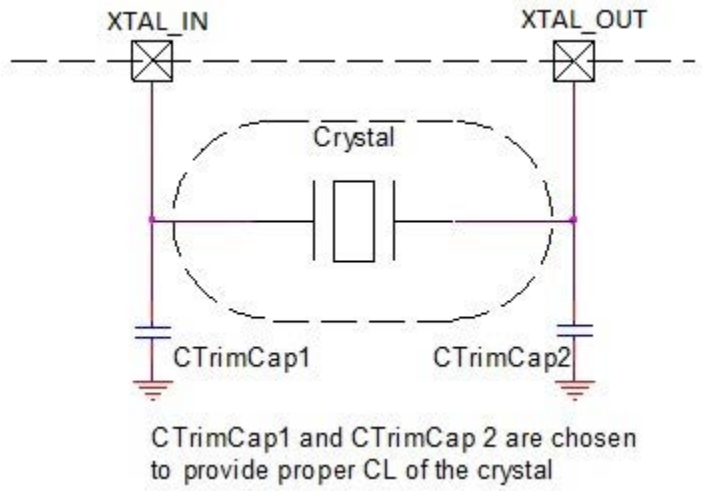
3.3 XTAL_IN/XTAL_OUT Timing

Table 32: Crystal Requirements

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)
Refer to Figure 14 for corresponding Symbol details.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	104-pin LFBGA Package	–	50	–	MHz
	Frequency Tolerance		-50	–	+50	ppm
	Target Frequency	48-pin QFN Package	–	25	–	MHz
	Frequency Tolerance		-50	–	+50	ppm
C_L	Load Capacitance	User Specified	–	6	12	pF
C_S	Shunt Capacitance	–	–	–	CL/6	pF
R_L or ESR	Equivalent Series Resistance	104-pin LFBGA Package C_L = 6 pF	–	–	60	Ω
		104-pin LFBGA Package C_L = 12 pF	–	–	40	Ω
		48-pin QFN Package C_L = 6 pF			100	Ω
		48-pin QFN Package C_L = 12 pF			100	Ω
D_L	Drive Level	–	100	–	–	µW

Figure 14: Crystal Reference Schematic

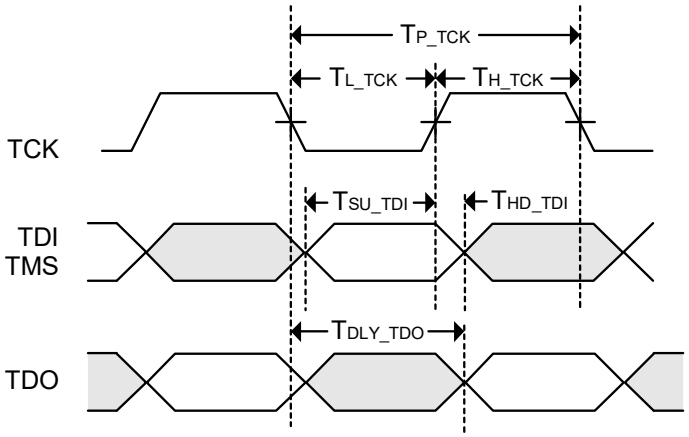


3.4 JTAG Timing

Table 33: JTAG Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	–	60	–	–	ns
T_{H_TCK}	TCK High	–	12	–	–	ns
T_{L_TCK}	TCK Low	–	12	–	–	ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	–	10	–	–	ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	–	10		–	ns
T_{DLY_TDO}	TCK to TDO Delay	–	0	–	15	ns

Figure 15: JTAG Timing



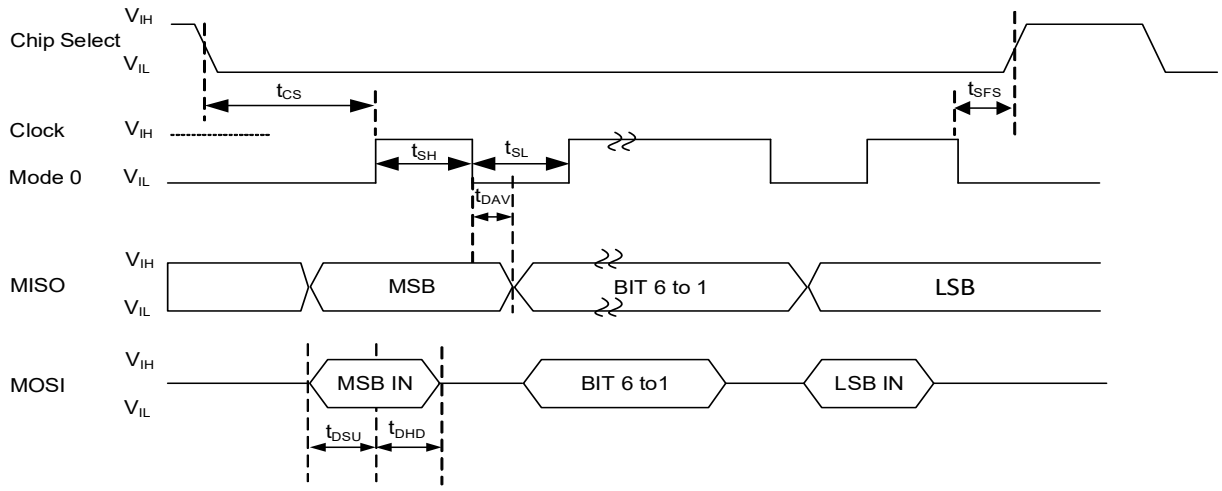
3.5 SPI Slave

Table 34: SPI Slave AC Characteristics

(Over full range of values listed in the Recommended Operating Conditions, unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f	Frequency	Mode 0	–	–	62.5	MHz
t_{CS}	Chip Select (CS) to Serial Clock (SCLK) Edge	–	16	–	–	ns
t_{SL}	SCLK Low Pulse Width	–	7.5	–	–	ns
t_{SH}	SCLK High Pulse Width	–	7.5	–	–	ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	–	4	–	–	ns
t_{DHD}	Data Input Hold Time After SCLK Edge	–	0	–	–	ns
$t_{D(W-R)}$	Write to Read Delay Time	–	100	–	–	ns
t_{DAV}	SCLK Data Output Valid	–	–	–	–	–
t_{SFS}	CS High After SCLK Edge	–	16	–	–	ns

Figure 16: SPI Slave Timing Diagram - Mode 0



3.6 SerDes

3.6.1 5GBASE-R

Table 35: 5GBASE-R Electrical Summary

Test Parameters	Specification			Units
Transmitter Tests				
	Min	**Typ**	**Max**	
Signaling Rate	-100 ppm	5.15625	+100 ppm	GBd
Nominal Unit Interval	–	193.9	–	ps
Deterministic Jitter	–	–	0.12	UI
Random Jitter	–	–	0.15	UI
Total Jitter Output	–	–	0.27	UI
Receiver Tests				
Signaling Rate	-100 ppm	5.15625	+100 ppm	GBd
Nominal Unit Interval	–	193.9	–	ps
Receiver Coupling	–	AC	–	N /A
Applied Random Jitter (min. peak-to-peak)	0.15	–	–	UI
Applied peak-to-peak Sinusoidal Jitter	0.115	–	–	UI
5GBASE-R Output DC Characteristics	**Min**	**Typ**	**Max**	**Units**
Differential Output	–	–	1200	mVpp

3.6.2 10G - XFI

Table 36: 10G - XFI Electrical Summary

Test Parameters	Specification			Units
Parameter	**Min**	**Typ**	**Max**	
Transmitter				
Reference Differential Impedance	–	100	–	Ω
Termination Mismatch	–	–	5	%
DC Common Mode Voltage	0	–	3.6	V
AC Common Mode Voltage	–	–	25	mV (RMS)
Differential Output Return Loss	SDD22 > 20 for 0.05-0.1GHz; SDD22 > 8 for 0.1-5.5GHz[1]	–	–	dB
Common Mode Output Return Loss	SCC22 > 3 for 0.1-12GHz[2]	–	–	dB
Total Jitter	–	–	0.61	UI
Total non-EQJ Jitter	–	–	0.41	UI
Transmitter Eye Mask[3]	–	see Figure 17	–	–
Eye Mask: X1	–	–	0.305	UI
Eye Mask: Y1	60	–	–	mV
Eye Mask: Y2	–	–	410	mV
Receiver Tests				
Reference Differential Impedance	–	100	–	Ω
Termination Mismatch	–	–	5	%
DC Common Mode Voltage	0	–	3.6	V
Input AC Common Mode Voltage	–	–	15	mV (RMS)
Differential Input Return Loss	SDD11 > 20 for 0.05-0.1GHz; SDD11 > 8 for 0.1-5.5GHz[1]	–	–	dB
Common Mode Input Return Loss	SCC11 > 3 for 0.1-12GHz[2]	–	–	dB
Differential to Common Mode Conversion	SCD11 >10 for 0.1-12GHz[2]	–	–	dB

Table 36: 10G - XFI Electrical Summary (Continued)

Test Parameters	Specification			Units
Parameter	**Min**	**Typ**	**Max**	
Receiver				
Total Jitter	–	–	0.34	UI
Deterministic Jitter	–	–	0.18	UI
Receiver Eye Mask[4]	–	see Figure 18	–	–
Eye Mask: X1	–	–	0.17	UI
Eye Mask: X2	–	–	0.42	UI
Eye Mask: Y1	170	–	–	mV
Eye Mask: Y2	–	–	425	mV

1. For Return Loss frequency from 5.5 - 12 GHz, Return Loss given by the equation SDD22(dB) = 8 - 20.66 Log10(f/5.5), with f in GHz
2. Common mode reference impedance is 25Ω. Common Mode Return Loss helps absorb reflections and EMI.
3. For Transmitter Eye Mask, refer to XFI specification, this is point B. As per XFI spec, point A and D are used as informative only.
4. For Receiver Eye Mask, refer to XFI specification, this is point C. As per XFI spec, point A and D are used as informative only.

Figure 17: Transmitter Differential Output Compliance Mask at Point B

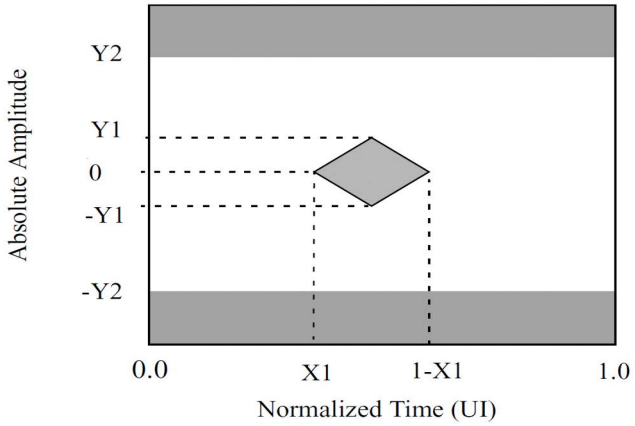
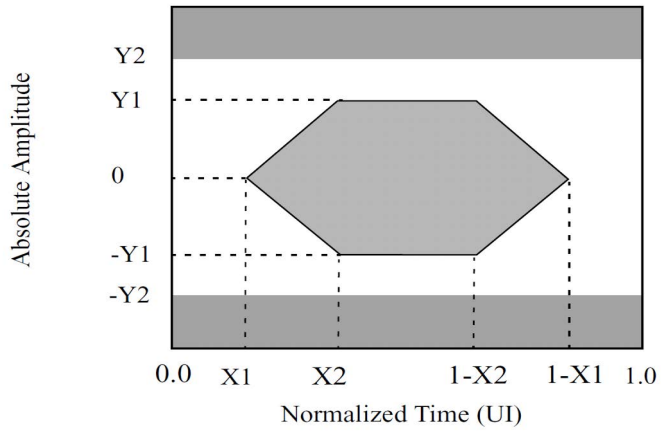


Figure 18: Receiver Differential Input Compliance Mask at Point C



3.6.3 2500BASE-X

Table 37: 2500BASE-X Electrical Summary

Test Parameters	Specification			Units
Transmitter Tests				
	Min	**Typ**	**Max**	
Signaling Rate	-100 ppm	3.125	+ 100 ppm	GBd
Nominal Unit Interval	–	320	–	ps
Deterministic Jitter	–	–	0.12	UI
Random Jitter	–	–	0.2	UI
Total Jitter Output	–	–	0.32	UI
Receiver Tests				
Signaling Rate	-100 ppm	3.125	+100 ppm	GBd
Nominal Unit Interval	–	320	–	ps
Receiver Coupling	–	AC	–	N/A
Differential Input peak-to-peak Amplitude	–	–	1200	mVpp
Applied Sinusoidal Jitter (min. peak-to-peak)	0.12	–	–	UI
Applied Random Jitter (min. peak-to-peak)	0.2	–	–	UI
2500BASE-X Output DC Characteristics	**Min**	**Typ**	**Max**	**Units**
Differential Output	800	1000	1200	mVpp

3.7 Latency Timing

3.7.1 Line Side Interface Latency Timing

- Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI.
- Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.
- The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 38: Device Latency vs. 802.3ch Delay Limits
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Mode	Interleave	Device Latency (ns)	802.3ch Delay Limits
2.5GBASE-T1	1x	3821.1	4096
5GBASE-T1	1x	1913.6	2048
5GBASE-T1	2x	2653.6	2764.8
10GBASE-T1	1x	962.6	1024
10GBASE-T1	2x	1332.6	1382.4
10GBASE-T1	4x	2053.6	2048

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 39: Power Supply Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Power Supply Voltage with Respect to VSS	Min	Typ	Max	Unit
AVDD12 and AVDDLS	–	–	1.32	V
AVDD33	–	–	3.63	V
AVDD08 and DVDD	–	–	0.88	V
VDDIO	–	–	3.63	V

Table 40: Absolute Maximum Ratings - Digital Pins

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Digital Pins	Min	Typ	Max	Unit
Voltage applied to any digital input pin	–	–	3.63 or VDDIO + 0.4, whichever is less	V

4.2 Recommended Operating Conditions

Table 41: Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
AVDD08	Input DC Voltage	0.815V	0.840V	0.865V	V
DVDD	Input DC Voltage	0.815V	0.840V	0.865V	V
AVDD12	Input DC Voltage	1.164V	1.200V	1.236V	V
	Voltage Ripple - peak-peak	–	–	12mV	V
AVDDLS	Input DC Voltage	1.164V	1.200V	1.236V	V
AVDD33	Input DC Voltage	3.201V	3.300V	3.399V	V
VDDIO @ 1.8V	Input DC Voltage	1.710	1.800V	1.890V	V
VDDIO @ 2.5V	Input DC Voltage	2.375V	2.500V	2.625V	V
VDDIO@ 3.3V	Input DC Voltage	3.135V	3.300V	3.465V	V

Table 41: Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
RSET	Internal bias reference Resistor connected to VSS	–	4990 ± 1% Tolerance	–	Ω
TA	Ambient operating temperature: Automotive Grade 2	-40	–	+105	°C
TJ	Junction temperature[1]	-40	–	140	°C

1. Operation beyond 125°C for extended periods may impact long term reliability. Care should be taken to ensure that the maximum operating junction temperature of 140°C is not exceeded in the System Design. Thermal mitigation measures should be taken if necessary.

Caution

Total measured DC + ripple must not exceed the input DC Voltages Min and Max range.

4.3 Power and Current Consumption

4.3.1 Steady-State Operating Conditions

Table 42: Typical Steady-State Operating Conditions

Symbol	Parameter	Test Condition	10G Line		5G Line	2.5G Line		Units
			10GBASE-R	10G USX	5GBASE-R/ 5G USX	10G USX	2500BASE-X	
$I_{VA12\ TOTAL}$	1.2V Input Current	Steady-State (typ)	191	191	155	157	157	mA
$I_{VA33\ TOTAL}$	3.3V Input Current	Steady-State (typ)	10	10	10	10	10	mA
$I_{DVDD\ TOTAL}$	0.84V Input Current (Digital)	Steady-State (typ)	497	500	249	181	164	mA
$I_{AVDD08\ TOTAL}$	0.84V Input Current (Analog)	Steady-State (typ)	41	41	40	40	40	mA
$I_{VDDIO\ TOTAL}$	VDDIO Input Current	Steady-State (typ)	7	7	7	7	7	mA
$P_{TOTAL_TYP_SS}$	Power	Steady-State (typ)	739	741	487	432	417	mW

NOTE: MACsec bypassed, 25°C, nom supplies, 1m cable

Table 43: Maximum Steady-State Operating Conditions

Symbol	Parameter	Test Condition	10G Line		5G Line	2.5G Line		Units
			10GBASE-R	10G USX	5GBASE-R/ 5G USX	10G USX	2500BASE-X	
$I_{VA12\ TOTAL}$	1.2V Input Current	Steady-State (max)	224	225	185	184	183	mA
$I_{VA33\ TOTAL}$	3.3V Input Current	Steady-State (max)	11	11	11	11	11	mA
$I_{DVDD\ TOTAL}$	0.84V Input Current (Digital)	Steady-State (max)	861	862	528	422	396	mA
$I_{AVDD08\ TOTAL}$	0.84V Input Current (Analog)	Steady-State (max)	63	63	62	72	71	mA
$I_{VDDIO\ TOTAL}$	VDDIO Input Current	Steady-State (max)	8	8	8	8	8	mA
$P_{TOTAL_MAX_SS}$	Power	Steady-State (max)	1165	1167	822	737	711	mW

NOTE: MACsec enabled, Tj = 140°C, +5% supplies, 15m cable

4.3.2 Low Power Mode Operating Conditions

Table 44: Maximum Power Low Power Mode

Symbol	Parameter	Test Condition	+/-5% Supplies, Tj = 140C	Unit
$I_{VA12\ TOTAL}$	1.2V Input Current	IEEE Low Power Mode (max)	82	mA
$I_{VA33\ TOTAL}$	3.3V Input Current	IEEE Low Power Mode (max)	11	mA
$I_{VDD\ TOTAL}$	0.84V Input Current	IEEE Low Power Mode (max)	261	mA
$I_{VDDIO\ TOTAL}$	VDDIO Input Current	IEEE Low Power Mode (max)	15	mA
$P_{TOTAL_TYP_SS}$	Power	IEEE Low Power Mode (max)	414	mW

4.4 Electrostatic Discharge (ESD) Ratings

Table 45: Electrostatic Discharge (ESD) Ratings

Parameter	I/O Pins	Value	Unit
Human Body Model (HBM)[1]	MDI pins	+/- 6	kV
	WAKE pin	+/- 6	kV
	All other pins	+/- 2	kV
Charged Device Model (CDM)[2]	Corner pins	+/- 750	V
	All other pins	+/- 500	V

1. Reference Standard - AEC-Q100, AEC-Q100-002

2. Reference Standard - AEC-Q100, AEC-Q100-011

4.5 Low Power Signal Detect (LPSD) Electrical Specifications

Table 46: LPSD Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	–	6	12	28	V
$I_{STANDBY}$	Standby current	Battery voltage = 12V	–	–	35	uA
$T_{MDI,LAT}$	Latency from MDI signals to INH assertion	–	–	–	1	ms
$T_{WAKE,PW}$	WAKE Pin Pulse Width to wake-up LPSD	–	40	–	–	µs
I_{INH}	INH Pin Source Current	V_{INH} = 1.9V with 10K Pull-down	–	–	0.23	mA
V_{INH}	INH Pin Output High Voltage	V_{INH} = 1.9V with 10K Pull-down	1.9	–	–	V
V_{IH_WAKE}	WAKE Pin Input High Voltage	–	1.87	–	–	V
V_{IL_WAKE}	WAKE Pin Input Low Voltage	–	–	–	0.5	V
V_{WAKE_OUT}	WAKE_OUT Pin Output Voltage	Case 1: Load 10K pull-down Case 2: Driving one or two WAKE_IN pin of BRIGHTLANE™ devices and 100K Pull-down resistor	1.9	–	–	V
VLPR	VLPR Pin Input Voltage	Externally supplied	2.7	3.3	3.465	V

4.6 Digital Pins

Table 47: Digital Pins
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

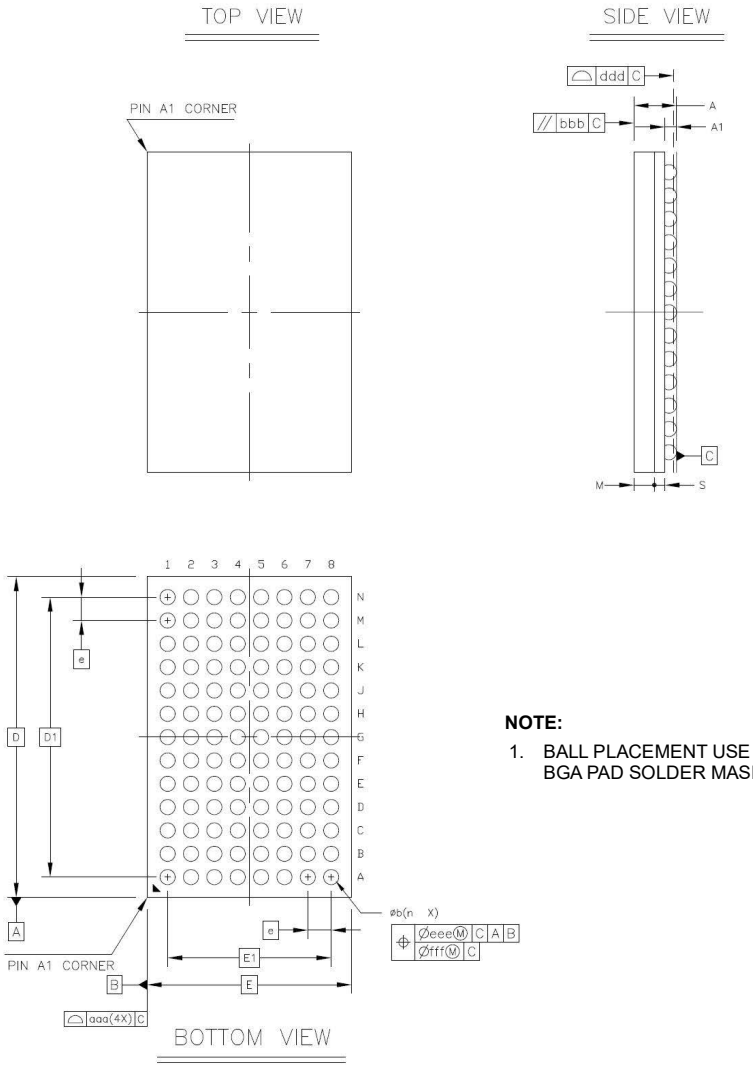
Symbol	Parameter	Pins	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	All digital inputs	VDDIO = 3.3V	2.31	–	VDDO + 0.4V	V
			VDDIO = 2.5V	1.75	–	VDDO + 0.4V	V
			VDDIO = 1.8V	1.26	–	VDDO + 0.4V	V
V_{IL}	Input low voltage	All digital inputs	VDDIO = 3.3V	-0.4	–	0.8	V
			VDDIO = 2.5V	-0.4	–	0.75	V
			VDDIO = 1.8V	-0.4	–	0.54	V
V_{OH}	High level output voltage	All digital outputs	–	VDDO - 0.4V	–	–	V
V_{OL}	Low level output voltage	All digital outputs	–	–	–	0.4	V
I_{ILK}	Input leakage current	–	–	–	–	10uA (for 0 < V(PAD) < VDDIO)	µA
C_{IN}	Input capacitance	LED	–	–	–	10	pF
		All pins except LED	–	–	–	5	pF

5 Package

5.1 Mechanical Drawings

5.1.1 104-Pin LFBGA Package

Figure 19: BRIGHTLANE™ Q324x 104-Pin LFBGA Package Mechanical Drawings



NOTE:

1. BALL PLACEMENT USE 0.50 mm SOLDER BALL
   BGA PAD SOLDER MASK OPENING = 0.40 mm

Table 48: 104-Pin LFBGA Package Dimensions

		Symbol	Dimension in mm		
			Min	Nom	Max
Body Size:	X	E	6.900	7.000	7.100
	Y	D	10.900	11.000	11.100
Ball Pitch:		e		0.800	
Total Thickness:		A	1.390	1.460	1.530
Mold Thickness:		M		0.700 Ref.	
Substrate Thickness:		S		0.360 Ref.	
Ball Diameter:				0.500	
Stand Off:		A1	0.350	0.400	0.450
Ball Width:		b	0.450	0.520	0.590
Package Edge Tolerance:		aaa		0.100	
TOP Parallelism:		bbb		0.200	
Coplanarity:		ddd		0.100	
Ball Offset (Package):		eee		0.150	
Ball Offset (Ball):		fff		0.080	
Ball Count:		n		104	
Edge Ball Center to Center:	X	E1		5.600	
	Y	D1		9.600	

5.1.2 Layout Considerations

Infineon recommends land pattern with pad size of 0.4 mm.

5.1.3 48-Pin QFN Package

Figure 20: BRIGHTLANE™ Q3241 48-Pin QFN Package Mechanical Drawings

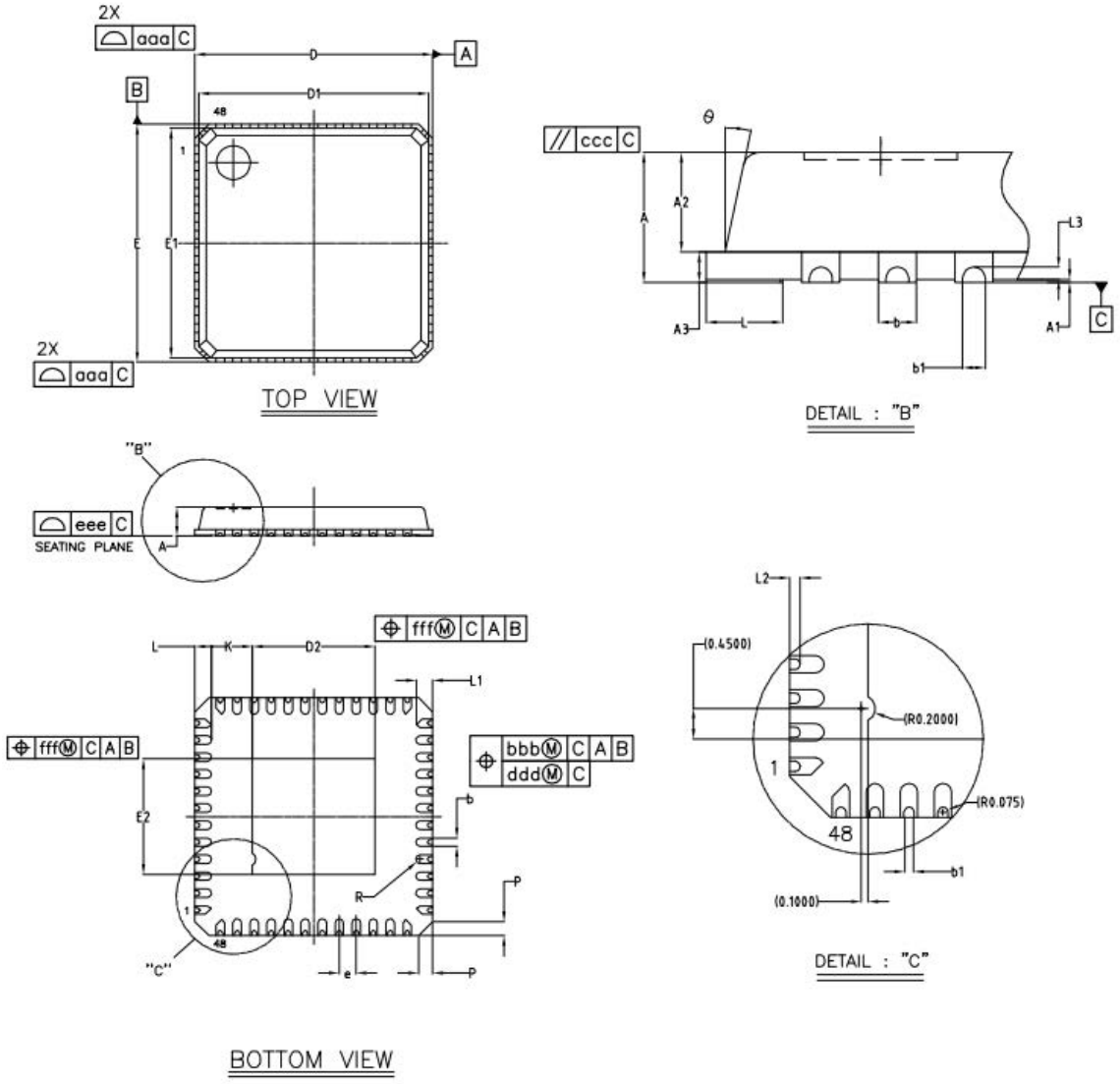


Table 49: 48-Pin QFN Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20 REF.	
b	0.18	0.25	0.30
b1	0.10	0.15	0.20
D	6.90	7.00	7.10
D1		6.75 BSC	
D2	3.50	3.60	3.70
E	6.90	7.00	7.10
E1		6.75 BSC	
E2	3.30	3.40	3.50
L	0.40	0.50	0.60
L1	0.387	0.487	0.587
L2	0.05	0.15	0.25
L3	0.05	0.10	0.15
P	0.24	0.42	0.60
e		0.500 BSC	
Θ	0°	--	14°
R	0.09	--	0.14
K	0.20	--	--
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Table 50: 48-Pin QFN Package Exposed Pad Size

Symbol	Dimension in mm		
	Min	Nom	Max
D2	3.500	3.600	3.700
E2	3.300	3.400	3.500

Note

- Controlling Dimension: Millimeter
- Reference Document: JEDEC MO-220

5.2 Package Thermal Information

5.2.1 104-pin LFBGA Package Thermal Information

Table 51: Thermal Conditions for 104-pin LFBGA Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	34.8	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	17.1	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	16.2	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	15.8	–	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	13.0	–	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	14.2	–	°C/W
ψ_{JB}	Junction-to-Board Thermal Characterization Parameter $\psi_{JB} = (T_J - T_{bottom})/P$ P = Total Power Dissipation T_{bottom} = Temperature on the Bottom of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	12.5	–	°C/W
ψ_{JT}	Junction-to-Top-Center Thermal Characterization Parameter $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation T_{top} = Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	2.5	–	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

5.2.2 48-Pin QFN Package Thermal Information

Table 52: Thermal Conditions for 48-Pin QFN Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-ambient thermal resistance $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	4 Layer JEDEC Board with no air flow	–	31.7	–	°C/W
		4 Layer JEDEC Board with 1 meter/sec air flow	–	20.9	–	°C/W
		4 Layer JEDEC Board with 2 meter/sec air flow	–	19.8	–	°C/W
		4 Layer JEDEC Board with 3 meter/sec air flow	–	19.3	–	°C/W
θ_{JB}	Junction-to-board thermal resistance $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface	4 Layer JEDEC Board with no air flow	–	11.9	–	°C/W
θ_{JC}	Junction-to-case thermal resistance $\theta_{JC} = (T_J - T_C) / P_{top}$ P_{top} = Power dissipation from the top of the package	4 Layer JEDEC Board with no air flow	–	13.6	–	°C/W
ψ_{JT}	Junction-to-top-center thermal characterization parameter $\psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation T_{top} = Temperature on the top center of the package	4 Layer JEDEC Board with no air flow	–	1.78	–	°C/W

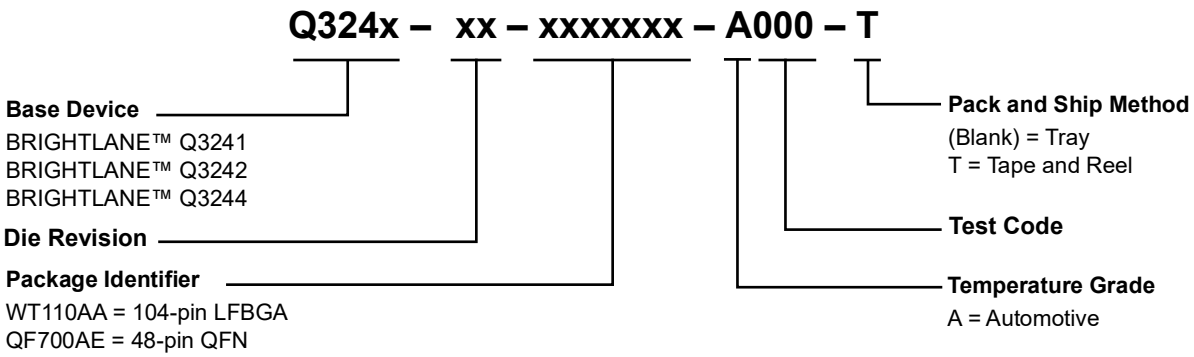
1. For more information, see θJC, θJA & Temperature Calculations, MV-S700019-00.

6 Ordering Part Number/Package Marking

6.1 Ordering Part Number

Figure 21 shows the ordering part numbering scheme for the BGA and QFN devices. Refer to the relevant release notes on the Infineon customer portal for the latest revision and complete part ordering information.

Figure 21: Sample Part Number



6.1.1 BRIGHTLANE™ Q324x 104-pin LFBGA Package Part Order Numbers

Table 53: BRIGHTLANE™ Q324x 104-pin LFBGA Package Part Order Numbers

Package Type	Part Order Number
104-pin LFBGA	Q3241-xx-WT110AA-A000 2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive)
104-pin LFBGA, Tape and Reel	Q3241-xx-WT110AA-A000-T 2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive, Tape and Reel)
104-pin LFBGA	Q3242-xx-WT110AA-A000 5G/2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive)
104-pin LFBGA, Tape and Reel	Q3242-xx-WT110AA-A000-T 5G/2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive, Tape and Reel)

Table 53: BRIGHTLANE™ Q324x 104-pin LFBGA Package Part Order Numbers (Continued)

Package Type	Part Order Number
104-pin LFBGA	Q3244-xx-WT110AA-A000 10G/5G/2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive)
104-pin LFBGA, Tape and Reel	Q3244-xx-WT110AA-A000-T 10G/5G/2.5G Base-T1 Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive, Tape and Reel)

6.1.2 BRIGHTLANE™ Q3241 48-pin QFN Package Part Order Numbers

Table 54: BRIGHTLANE™ Q3241 48-pin QFN Package Part Order Numbers

Package Type	Part Order Number
48-Pin QFN	Q3241-xx-QF700AE-A000 2.5G Single Port 802.3ch Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive)
48-Pin QFN, Tape and Reel	Q3241-xx-QF700AE-A000-T 2.5G Single Port 802.3ch Automotive PHY (Green, RoHS 6/6 and Halogen-free package, Automotive, Tape and Reel)

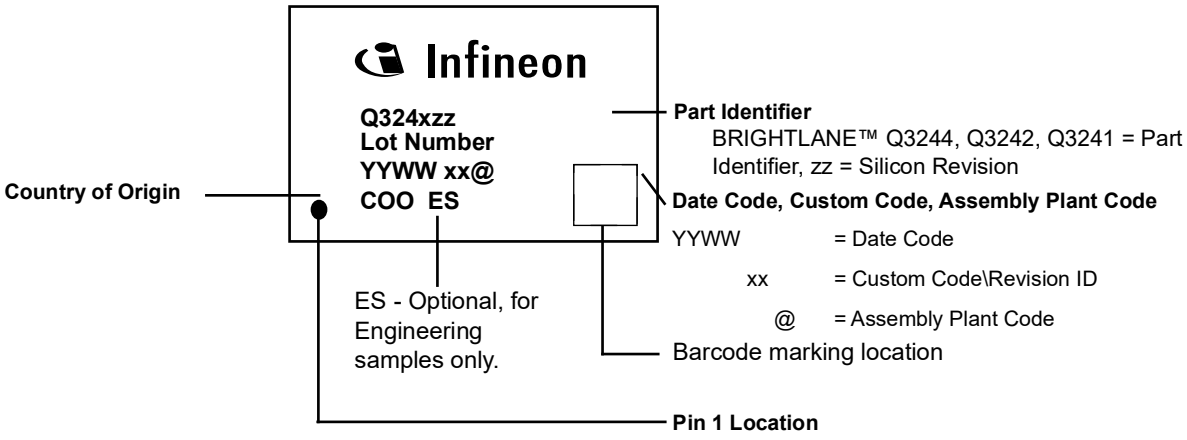
6.2 Package Marking

Customers may receive products with either Marvell or Infineon branding due to the transition, although the devices remain functional equivalents.

6.2.1 BRIGHTLANE™ Q3244/Q3242/Q3241 104-pin LFBGA Package Marking

Figure 22 shows a sample package marking and pin 1 location for the BRIGHTLANE™ Q3244/Q3242/Q3241 104-pin LFBGA package (Automotive, Green).

Figure 22: BRIGHTLANE™ Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location – Automotive Grade 2

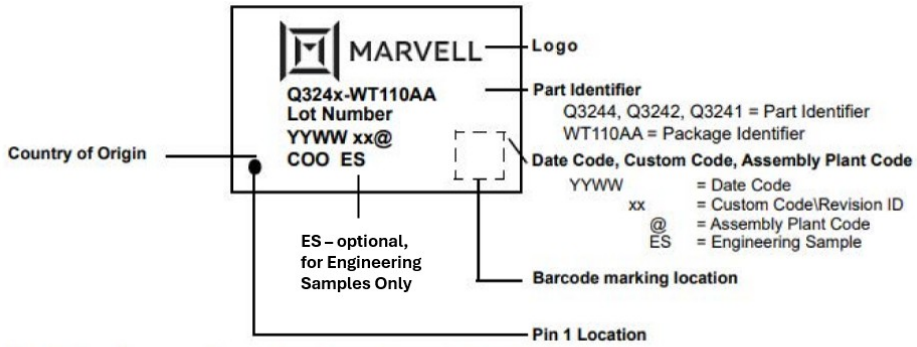


Note: The above example is not drawn to scale. Location of markings is approximate.

6.2.2 MV-Q3244/MV-Q3242/MV-Q3241 104-pin LFBGA Package Marking

Figure 23 shows a sample package marking and pin 1 location for the MV-Q3244/MV-Q3242/MV-Q3241 104-pin LFBGA package (Automotive, Green).

Figure 23: MV-Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location – Automotive Grade 2

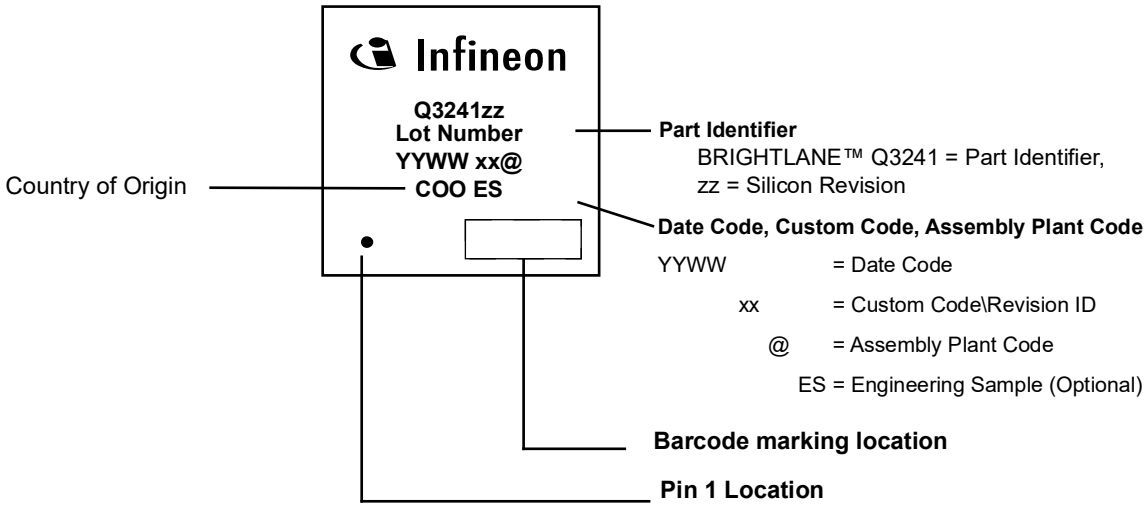


Note: The above example is not drawn to scale. Location of markings is approximate.

6.2.3 BRIGHTLANE™ Q3241 48-pin QFN Package Marking

Figure 24 shows a sample package marking and pin 1 location for the BRIGHTLANE™ Q3241 48-Pin QFN package (Automotive, Green).

Figure 24: BRIGHTLANE™ Q3241 48-pin QFN Sample Package Marking and Pin 1 Location – Automotive Grade 2

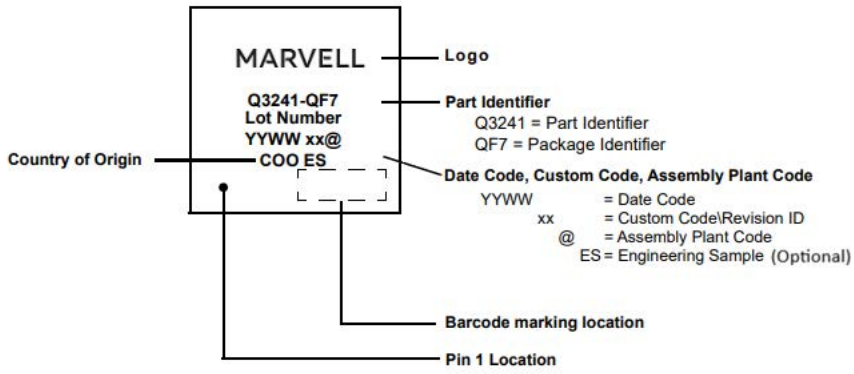


Note: The above example is not drawn to scale. Location of markings is approximate.

6.2.4 MV-Q3241 48-pin QFN Package Marking

Figure 25 shows a sample package marking and pin 1 location for the MV-Q3241 48-Pin QFN package (Automotive, Green).

Figure 25: MV-Q3241 48-pin QFN Sample Package Marking and Pin 1 Location – Automotive Grade 2



Note: The above example is not drawn to scale. Location of markings is approximate.

A Revision History

Table 55: Revision History

Revision	Date	Description
Rev. 12	March 31, 2026	• Updated Figure 20, BRIGHTLANE™ Q3241 48-Pin QFN Package Mechanical Drawings, on page 66 and Table 49, 48-Pin QFN Package Dimensions, on page 67.
Rev. 11	March 26, 2026	• Updated Figure 22, BRIGHTLANE™ Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location – Automotive Grade 2, on page 73 and Figure 24, BRIGHTLANE™ Q3241 48-pin QFN Sample Package Marking and Pin 1 Location – Automotive Grade 2, on page 75.
Rev. 10	March 16, 2026	• Updated description of INTn pin in Table 22, Interrupt, on page 40. • Added Figure 23, MV-Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location – Automotive Grade 2, on page 74 and Figure 25, MV-Q3241 48-pin QFN Sample Package Marking and Pin 1 Location – Automotive Grade 2, on page 76. • Changed the status of INTn functional block from “Off-floating” to “Disable” under Open Alliance Sleep in Table 8, Status of Functional Block in Each Mode, on page 23. • Updated the description in Section 1.6, Interrupts, on page 18.
Rev. 09	January 20, 2026	Updated Table 12.
Rev. 08	October 28, 2025	Migrated to Infineon template
Rev. 07	June 12, 2025	Datasheet release.
	June 5, 2025	Table 19: Clock/Configuration/Management/PTP/Reset/IO - Pin J8/37 - SPI_ CSn - added BGA and QFN details Table 29: Dual-function Pins for QFN Package - Pin # 37, updated Primary Purpose and deleted GPIO2 from Alt1 Purpose. Table 32: Crystal Requirements - Symbol RL or ESR - added 104-pin LFBGA and 48-pin QFN details.
	March 11, 2025	Section 1.2.1, System Interface Features and Modes - second paragraph, removed ‘, 2.5GBASE-X’ Section 1.8.1.1, PHYAD (PHY Address) - fourth paragraph, removed ‘2.5GBASE-X and’
	March 5, 2025	Section 3.6.2, 10G - XFI - changed section title to 10G - XFI Electrical Summary Table 36: 10G - XFI Electrical Summary - changed table title to 10G - XFI Electrical summary. Table heading, second row changed from Transmitter Tests to Receiver Tests. Added footnote 3 to Transmitter Eye Mask row and footnote 4 to Receiver Eye Mask row. Figure 17 title changed from Transmitter Differential Output to Receiver Differential Input Compliance Mask Removed Figure 18: Receiver Input Sinusoidal Jitter Tolerance Figure 19: title changed from Receiver Differential Input to Transmitter Differential Output Compliance Mask

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 06	January 17, 2025	Datasheet release.
		Features, General bullet items, Multi-speed SerDes, removed 2.5GBASE-X
		Table 1: Q3241/Q3242/Q3244 Device Features - removed rows 2.5GBASE-X (Clause 27), 5000 BASE-R (Clause 49) and combined rows 10GBASE-R (Clause 49)/XFI
		Figure 1: BRIGHTLANE™ Q3241/Q3242/Q3244 BGA Device Block Diagram and Figure 2: BRIGHTLANE™ Q3241QFN Device Block Diagram - removed 2.5GBASE-X and corrected Connector spelling
		Section 1.1.3, Automatic Polarity Detection and Correction, section rewrite
		Section 1.2.1, System Interface Features and Modes - System Interface features bullet items, removed 2.5GGBASE-X (Clause 127) and 5000 BASE-R (Clause 49) and removed paragraph and reference. Table 2: Modes - removed 2.5G/ Table 3: IPG Requirements - removed 2.5GBASE-X row Section , 2500BASE-X False Carrier Errors heading, removed 2.5GBASE-X

Revision History

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 06 (Cont.)	January 17, 2025	Table 4: PCS Modes - removed CFG_MODE 010 Table 5: USXGMII Single Port Options - removed 5000GBASE-R Table 6: System Interface MDIO Registers LSB 0xA000 and 0xB000 removed 2.5GBase-X and Exernal column Section 1.2.6, System Interface PRBS Testing, section rewrite
		Figure 5: Low Power Signal Detect (LPSD) Block Diagram - Option 1 and Figure 6: Low Power Signal Detect (LPSD) Block Diagram - Option 2 changed WAKE_IN to WAKE and removed 'Preliminary' from each title.
		LPSD Application Notes - item d., removed 'If on-chip regulator not used..."
		Section 1.7.1.3, Sleep/Wake-up through Section 1.7.1.5, Wake-Up Pulse - rewrote sections
		Section 1.7.2, Power Supply Sequencing - second paragraph, added 'when TC10 is used' Table 32: Crystal Requirements - updated Symbol R_L or ESR with C_L = 6 pF and C_L = 12 pF Conditions and values.
		Table 10: Configuration for Firmware Boot Source, MDIO vs. SPI Mode - added footnote 2 to Flash
		Table 12: Mode Configuration CONFIG4 Value 1 CONFIG3 Value 1 System Config removed 2.5G and CONFIG4 Value CONFIG3 Value 1 removed 2.5G
		Table 34: SPI Slave AC Characteristics - added Condition Mode 0 Figure 16: SPI Slave Timing Diagram - Mode 0, removed Mode 2 Removed Figure 17: SPI Slave Timing Diagram - Mode 1 and Mode 3 and Figure 18: Register Read Timing Example
		Table 35: 5GBASE-R Electrical Summary - Test Parameters - Applied peak-to-peak Sinusoidal Jitter - removed rows to only include 0.115 UI under Min
		Section 3.6.2, 10G - XFI - updated complete section and figures
		Table 37: 2500BASE-X Electrical Summary - Updated Deterministic Jitter, Random Jitter, Total Jitter Output, Differential Input peak-to-peak Amplitude, Applied Sinusoidal Jitter (min. peak-to-peak), and Applied Random Jitter (min. peak-to-peak) values
		Table 41: Recommended Operating Conditions - Symbol T_J, added footnote "Operation beyond 125°C for extended periods may impact long term reliability.".
		Updated Table 42: Typical Steady-State Operating Conditions and Table 43: Maximum Steady-State Operating Conditions values
		Table 46: LPSD Electrical Characteristics - updated values
		Figure 23: BRIGHTLANE™ Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location - Automotive Grade 2- added Barcode marking details.
Rev. 05	December 6, 2024	Datasheet release.
	November 13, 2024	Table 1: Q3241/Q3242/Q3244 Device Features - Line Interface 2.5GBASE-T1, removed System Interface row 10G USXGMII (2.5G/5/10G wire speeds) and Line Interface 5GBASE-T1, removed 2.5 from row 5G USXGMII (2.5/5G wire speeds)
	November 11, 2024	Datasheet updated from Preliminary to Final status.

Revision History

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 04	October 18, 2024	Datasheet release.
	October 10, 2024	Table 36: 10G - XFI Electrical Summary - Differential Output from TBD to 1200 Table 44: Maximum Power Low Power Mode - added Units column
	September 25, 2024	Updated Section 1.7.2, Power Supply Sequencing and Section 4.3, Power and Current Consumption details
Rev. 04 (Cont.)	September 25, 2024	Table 31: Reset Timing - Symbol $T_{SU_XTAL_IN}$ Min value 1 changed to 10 Table 39: Power Supply Absolute Maximum Ratings - row AVDD12 - added AVDDLS
	August 22, 2024	Section 2.9.3, SerDes Loopback removed section. Figure 23: BRIGHTLANE™ Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location - Automotive Grade 2- markings left justified and added Barcode marking details.
	August 5, 2024	Table 19: Clock/Configuration/Management/PTP/Reset/IO - BGA Pin J1/QFN Pin 21 XTAL_IN, removed sentence 'XTAL_IN must AC coupled with capacitor to AVSS.', and BGA Pin H1/QFN Pin 20 XTAL_OUT, removed sentence 'XTAL_OUT must AC coupled with capacitor to AVSS.'.
	July 18, 2024	Table 19: Clock/Configuration/Management/PTP/Reset/IO - Pin A3 FLASH_CEN, removed sentence 'For normal operation, connect VSS to 4.7kΩ resistor'.

Revision History

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 03	July 12, 2024	Datasheet release.
	June 26, 2024	Section 1.7.2, Power Supply Sequencing - first sentence, changed 2 ms to 4 ms, and 'rail to rail' to 'first rail to last rail'
		Table 45: Electrostatic Discharge (ESD) Ratings - removed footnote 3
	June 17, 2024	Section , LPSD Application Notes - changed item a. from 'If WAKE bus is running on 3.3V supply' to 'If WAKE bus is running less than or equal to 3.3V supply', and changed item b. 50 kΩ to 25 kΩ
	June 3, 2024	Removed Section 4.1.1, 10G USXGMII Input AC Characteristics
	May 6, 2024	Table 25: Power and Ground AVDD08 and DVDD changed from 0.8V to 0.84V Section 1.7, Power Supplies and Management, 0.8V changed to 0.84V throughout section. Table 41: Recommended Operating Conditions AVDD08 and DVDD changed from 0.80V to 0.84V with +/-3% for max and min respectively Section 4.3, Power and Current Consumption, 0.8V changed to 0.84V throughout section
	April 29, 2024	Figure 23: BRIGHTLANE™ Q3241 48-pin QFN Sample Package Marking and Pin 1 Location - Automotive Grade 2 added Package Identifier details
	April 15, 2024	Table 31: Reset Timing - Symbol T_{PU_RESET} Min value 10 changed to 1 and Unit from μσ to ms
	April 2, 2024	Table 41: Recommended Operating Conditions - updated VDDIO Min and Max values
	March 8, 2024	Added Q3241 48-pin QFN package details and updated applicable package differences throughout datasheet. Updated Figure 1: BRIGHTLANE™ Q3241/Q3242/Q3244 BGA Device Block Diagram Updated Figure 22: BRIGHTLANE™ Q324x 104-pin LFBGA Sample Package Marking and Pin 1 Location - Automotive Grade 2 to represent actual package marking
	February 23, 2024	Table 19: Clock/Configuration/Management/PTP/Reset/IO - Pin C3 updated name and definition to CONFIG3/FLASH_SI, Pin C2 CONFIG4/FLASH_SO updated name and definition, Pin A3 changed from Reserved (Pull low) to FLASH_CEN, Pin H8 updated name to SPI_MISO/CONFIG_OUT1, Pin B3 updated name to PTP_TRIG_IN/FLASH_SCK and updated definition. Table 23: LED - Pin K3 updated name to LED/CONFIG_OUT0 Table 27: Reserved and No Connect Pins - Pin A3 changed and moved to Table 19 Updated attached Q3241_ Q3242_ Q3244 BGA Pinout and Pin List with changes above. Table 15: BRIGHTLANE™ Q324x Boundary Scam Chain - added Scan Chain order pins Table 19: Clock/Configuration/Management/PTP/Reset/IO - updated pin J1, XTAL_IN and pin H1, XTAL_OUT definitions Table 41: Recommended Operating Conditions removed all Voltage Ripple except AVDD. AVDD added peak-peak to voltage ripple and Max value to 12mV.

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 03 (Cont.)	January 29, 2024	Added Table 1: Q3241/Q3242/Q3244 Device Features.
	January 23, 2024	Table 36: 10G - XFI Electrical Summary - removed row - 10GBASE-R Output DC Characteristics
		Updated Table 42: Typical Steady-State Operating Conditions and Table 43: Maximum Steady-State Operating Conditions

Revision History

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 02	December 22, 2023	Datasheet release.
	December 15, 2023	Timings - Added Cs, RL or ESR and DL rows to Table 32: Crystal Requirements - Added Section 3.5, SPI Slave - Added Section 3.6, SerDes
	December 11, 2023	Features - Updated Features text, General and Compliance details, added device differences Table 24: Clock/Configuration/Management/PTP/Reset/IO, and where applicable - Removed SPI Flash from section and table headings - Pin A3 changed from SLEEP_DIS/FLASH_CEN to Reserved (Pull Low)
		- Pin B3 changed from PTP_TRIG_IN/FLASH_SCK to - PTP_TRIG_IN - Pin C3 changed from CONFIG3/FLASH_SI to CONFIG3 - Pin C2 changed from CONFIG4/FLASH_SO to CONFIG4 Section 1.7.4, Transitions of Each Mode - third bullet added '(UV)' Figure 8: Transitions in each mode updated for single port example Section 1.8.1, Hardware Configuration - second sentence, removed 'flash and', added paragraph before Table 12: Mode Configuration and removed Note Section 1.10.1, SPI Slave Interface - updated section title to SPI Slave Interface, removed SPI Flash Interface Block Diagram Section 1.11, Precision Time Protocol (PTP) Time Stamping Support - third paragraph - removed first sentence "The PTP core..." Section 4.1, Host Interface Timing - changed title to Host Interface Timing Removed Section 5.3.3 Instantaneous Current Conditions
	November 9, 2023	Table 26: Low Power Signal Detect - Pin A6, VLPR, updated definition, and added Symbol VLPR and details to Table 46: LPSD Electrical Characteristics
	November 03, 2023	Updated Figure 3: Functional Block Diagram to identify Line and System Interface external signal connections
		Figure 22: BRIGHTLANE™ Q324x 104-pin LFBGA Sample Packing Marking and Pin 1 Location - Automotive Grade 2 added ES and zz details
		Typo correction 80.23ch to 802.3ch, throughout
		Added Section 1.7.2, Power Supply Sequencing
		Table 41: Recommended Operating Conditions - updated table to merge details with Table 50: Electrical Parameters, updated CAUTION below table
	August 29, 2023	Table 42: Typical Steady-State Operating Conditions and Table 43: Maximum Steady-State Operating Conditions, updated table heading 2.5G (USX) to 10G (USX) and added all values
		Added Section 4.4, Electrostatic Discharge (ESD) Ratings
	August 16, 2023	25 MHz clock support to 50 MHz, throughout
	July 19, 2023	Section 1.7.1.2, Open Alliance TC10 Sleep Mode - LPSD Application Notes - Case 4, VLPR changed to VLPR = 3.3V

Revision History

Table 55: Revision History (Continued)

Revision	Date	Description
Rev. 02 (Cont.)	July 13, 2023	Added Section 1.13, IEEE 1149.1 and 1149.6 Controller
	June 14, 2023	Table 27: Reserved and No Connect Pins - Pin K4 (Reserved, Pull Low) changed to TEST_SEL and moved to Table 20: JTAG/Test Pins
	May 5, 2023	Figure 19: BRIGHTLANE™ Q324x 104-Pin LFBGA Package Mechanical Drawings - added NOTE regarding Ball Placement and Solder Mask Table 30: MDC/MDIO Timing, TP_RISE and TP_FALL Min 6 ns values corrected to Max 6 ns
	April 25, 2023	Section 5.1.2, Layout Considerations - added section
	April 17, 2023	Section 2.1, Copper Media Interface name changed to Copper Media Dependent Interface (MDI), and complete update of section Section 1.3, Resets, first paragraph, added reference to Reset Timing Table 31: Reset Timing, added T_{PU_RESET} Min value 10 us
	March 30, 2023	Added Q3241 and Q3242 product details. Updated Figure 1: Q3241/Q3242/Q3244 BGA Device Block Diagram to include all devices Section 1.2, System Interface, complete update of section Section 1.4, Undervoltage (UV) Detection, moved to separate section, added '(UV)' to section title and 'Undervoltage' to last sentence, added AVDD08 Section 1.7, Power Supplies and Management, first paragraph, updated last sentence Section 1.9.2, Loopbacks - added SerDes Loopback details, updated all figures Figure 5: Low Power Signal Detect (LPSD) Block Diagram - Option 1 and Figure 6: Low Power Signal Detect (LPSD) Block Diagram - Option 2, added 2.5G/5G/10GBASE-T1 to each PHY block and added product numbers. Table 8: Status of Functional Block in Each Mode, updated conditions for each mode to Disable, Functional, etc. Previous section heading Section 4.3 Latency Timing moved to standalone Section 3.7, Latency Timing
	December 13, 2022	Added Section 5.2, Package Thermal Information for 104-Pin LFBGA package
	December 7, 2022	Figure 5: Low Power Signal Detect (LPSD) Block Diagram - Option 1 - updated Q1 to Darlington bipolar
Rev. 01	October 17, 2022	Initial version.

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